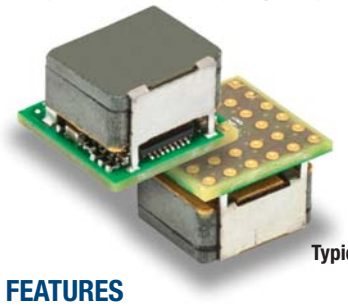
Murata Power Solutions

Okami™ OKDL-T/18-W12-xxx-C

18A Digital PoL DC-DC Converter Series

PRELIMINARY



Typical unit

FEATURES

- Small package: 12.2 x 12.2 x 8.0 mm (0.48 x 0.48 x 0.315 in)
- 0.6 V - 1.8 V output voltage range
- High efficiency, typ. 91.6% at 12Vin, 1.8Vout and 50% load
- Configuration Control and Monitoring via PMBus
- Adaptive compensation of PWM control loop & fast loop transient response
- Synchonization input & phase spreading/interleaving
- Voltage Tracking & Voltage margining
- MTBF 24 Mh
- For narrow board pitch applications (15 mm/0.6 in)
- Pre-bias start-up & shut down
- Monotonic & Soft start Power up
- Input under voltage shutdown; OTP, output OVP, OCP
- Remote control & Power Good
- Differential sense pins
- Voltage setting via pin-strap or PMBus
- Advanced Configurable via Graphical User Interface
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

PRODUCT OVERVIEW

TBD

Applications

- Distributed power architectures
- Intermediate bus voltage applications
- Servers and storage applications
- Network equipment

PART NUMBER STRUCTURE

OKD L - T / 18 - W12 - xxx - C

- **OKD** — **Digital Non-isolated PoL**
- **L** — **LGA Package**
- **T** — **Trimmable Output** Voltage Range 0.6 - 1.8Vdc
- **18** — **Maximum Rated Output** Current in Amps
- **W12** — **Input Voltage Range** 4.5-14Vdc
- **xxx** — **Software Configuration Digits** (001 is positive turn-on logic)
- **C** — **RoHS Hazardous Substance Compliance** **C** = RoHS-6 (does not claim EU RoHS exemption 7b – lead in solder)

RoHS COMPLIANT

c UL us

PMBus

ORDERING GUIDE	
Model Number	Output
OKDL-T/18-W12-001-C	0.6-1.8 V, 18 A/ 36 W

Absolute Maximum Ratings

Characteristics		Min	Typ	Max	Unit
T_{P1}	Operating temperature (see Thermal Consideration section)	-40		120	°C
T_S	Storage temperature	-40		125	°C
V_I	Input voltage (See Operating Information Section for input and output voltage relations)	-0.3		18	V
Logic I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, PG, CS_VTRK	-0.3		4	V
Ground voltage differential	-S, PREF, GND	-0.3		0.3	V
Analog pin voltage	VO, +S	-0.3		5.5	V

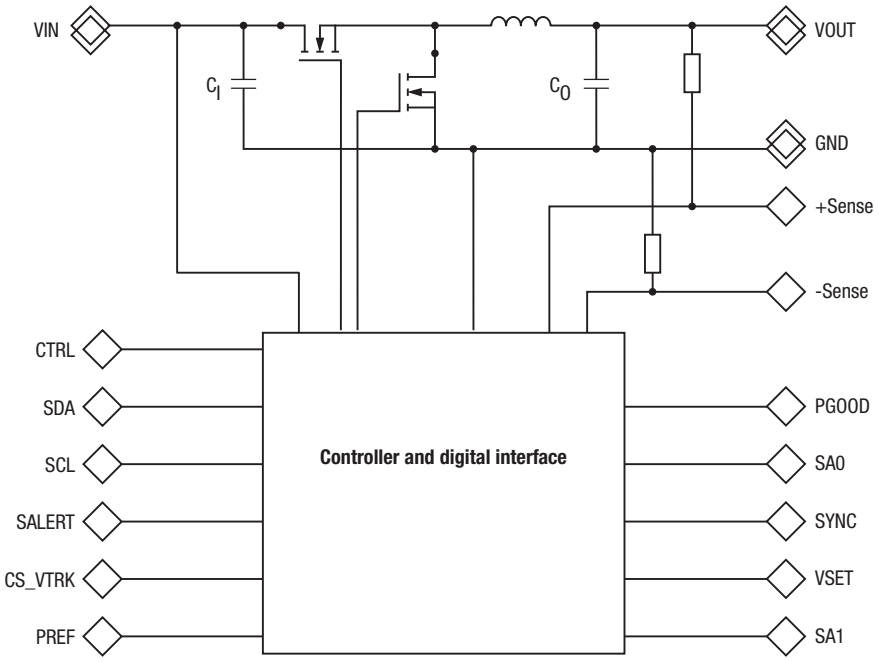
General and Safety	Conditions	Min	Typ	Max	Unit
Safety	Designed for UL/IEC/EN 60950 1				
Calculated MTBF	Telcordia SR-332, Issue 2 Method 1		14.2		Mhrs

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the default configuration file, unless otherwise specified. The default configuration file is designed to fit most application needs with focus on high efficiency. If different characteristics are required it is possible to change the configuration file to optimize certain performance characteristics.

In this Technical specification examples are included to show the possibilities with digital control. See Operating Information section for information about trade offs when optimizing certain key performance characteristics.



Fundamental Circuit Diagram

Electrical Specifications

T_{P1} = -30 to +95°C, VI = 4.5 to 14 V, VI > VO + 1.0 V
Typical values given at: TP1 = +25°C, VI = 12.0 V, max IO, unless otherwise specified under Conditions.
Default configuration file, 190 10-CDA 102 0519/001. VO defined by pin strap.
External CIN = 47 µF ceramic + 270 µF/10 mΩ electrolytic, COUT = 3x100 µF + 0.1 µF ceramic.
See Operating Information section for selection of capacitor types. Sense pins are connected to the output pins.

Characteristics			Conditions	Min	Typ	Max	Unit
V_I	Input voltage			4.5		14	V
V_O	Output voltage without pin strap				0		V
	Output voltage adjustment range			0.60		1.8	V
	Output voltage adjustment including PMBus margining			0.50		2.0	V
	Output voltage set-point resolution				1.2		mV
	Output voltage accuracy		Including line, load, temp	-1		1	% V_O
	Internal resistance +S/-S to VOUT/GND				47		Ω
	+S bias current				50		µA
	-S bias current				-35		µA
	Line regulation	I_O = max I_O	V_O = 0.6 V		3		mV
			V_O = 1.2 V		3		
			V_O = 1.8 V		5		
	Load regulation	I_O = 0 - 100%	V_O = 0.6 V		2		mV
			V_O = 1.2 V		2		
			V_O = 1.8 V		1		
V_{Oac}	Output ripple & noise (up to 20 MHz)		V_O = 0.6 V		10		mVp-p
			V_O = 1.2 V		10		
			V_O = 1.8 V		11		
I_O	Output current			0		18	A
I_S	Static input current at max I_O		V_O = 0.6 V		0.38		A
			V_O = 1.2 V		0.70		
			V_O = 1.8 V		1.00		
I_{lim}	Current limit threshold				22	23	A
I_{sc}	Short circuit current		RMS, hiccup mode, V_O = 3.3 V, 4 mΩ short		3		A
η	Efficiency	50% of max I_O	V_O = 0.6 V		81.0		%
			V_O = 1.2 V		88.7		
			V_O = 1.8 V		91.6		
		I_O = max I_O	V_O = 0.6 V		79.3		%
			V_O = 1.2 V		87.5		
			V_O = 1.8 V		90.5		
d	Power disipation at max I_O		V_O = 0.6 V		2.80		W
			V_O = 1.2 V		3.10		
			V_O = 1.8 V		3.40		
P_{li}	Input idling power	I_O = 0	V_O = 0.6 V		0.70		W
			V_O = 1.2 V		0.70		
			V_O = 1.8 V		0.71		
P_{CTRL}	Input standby power		Turned off with CTRL-pin		0.25		W
C_I	Internal input capacitance		V_I = 0 V		47		µF
C_O	Internal output capacitance		V_O = 0 V		47		µF
			V_O =1.2 V		39		
			V_O = 1.8 V		35		
C_{OUT}	Total output capacitance		Effective capacitance. Note 1	55			µF
V_{tr1}	Load transient peak voltage deviation		Load step 25-75-25% of max I_O, di/dt = 1.5 A/µs C_O=3x100 µF + 270 µF V_O = 1.8 V		70		mV
t_{tr1}	Load transient recovery time				22		µs
F_{sw}	Switching frequency				600		kHz
	Switching frequency range		PMBus configurable FREQUENCY_SWITCH. Note 2		300-1000		kHz
	Switching frequency set-point accuracy			-10	±5	10	%
	External Sync Duty Cycle			40		60	%
	Input Clock Frequency Drift Tolerance		External clock source	-10		10	%

Characteristics		Conditions	Min	Typ	Max	Unit
Input Under Voltage Lockout (hardware controlled)	Threshold, V_{UVLO}	Rising edge	3.8	4.1	4.4	V
	Hysteresis			0.24		V
Input Over Voltage Lockout (hardware controlled)	Threshold, V_{OVLO}	Input rising	14.3	15.2	16	V
Input Turn-On Voltage	Threshold			4.35		V
	Threshold range	PMBus configurable VIN_ON		0-14.7		V
Input Turn-Off Voltage	Threshold			3.8		V
	Threshold range	PMBus configurable VIN_OFF		0-14.7		V
Input Under/Over Voltage Protection, IUVP/ IOVP	IUVP threshold			4.1		V
	IUVP threshold range	PMBus configurable VIN_UV_FAULT_LIMIT		0-14.7		V
	IOVP threshold			14.4		V
	IOVP threshold range	PMBus configurable VIN_OV_FAULT_LIMIT		0-14.7		V
	Set point accuracy		-150		150	mV
	Fault response	VIN_UV_FAULT_RESPONSE VIN_OV_FAULT_RESPONSE	Shutdown, make continuous restarts at 700 ms interval (hiccup). Note 3			
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_0
	UVP threshold range	PMBus configurable VOUT_UV_FAULT_LIMIT		0-100		% V_0
	OVP threshold			115		% V_0
	OVP threshold range	PMBus configurable VOUT_OV_FAULT_LIMIT		100-115		% V_0
	Fault response	VOUT_UV_FAULT_RESPONSE VOUT_OV_FAULT_RESPONSE	Shutdown, make continuous restarts at 700 ms interval (hiccup). Note 3			
Over Current Protection, OCP	OCP threshold	Set value		24		A
	OCP threshold range	PMBus configurable IOUT_OC_FAULT_LIMIT		0-24		A
	Fault response	IOUT_OC_FAULT_RESPONSE	Shutdown, make continuous restarts at 700 ms interval (hiccup). Note 3.			
Over Temperature Protection, OTP	OTP threshold	Note 4		120		°C
	OTP threshold range	PMBus configurable OT_FAULT_LIMIT		-40…+120		°C
	OTP hysteresis	PMBus configurable		15		°C
	Fault response	OT_FAULT_RESPONSE	Shutdown, make continuous restarts at 700 ms interval (hiccup). Note 3			
Over Temperature Shutdown (hardware controlled)	Threshold	Note 4		150		°C
	Hysteresis			20		°C
	Accuracy			±20		°C

V_{OL}	Logic output low signal level	SCL, SDA, SYNC, SALERT, PG Sink/source current = 4 mA			0.4	V
V_{OH}	Logic output high signal level		2.8			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				4	mA
V_{IL}	Logic input low threshold	SCL, SDA, CTRL, SYNC			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL_CTRL}	Logic input low sink current	CTRL			0.5	mA
I_{I_LEAK}	Logic leakage current	SCL, SDA, SYNC, SALERT, PG			10	uA
f_{SMB}	SMBus Operating frequency			400		kHz
T_{BUF}	SMBus Bus free time	STOP bit to START bit See section SMBus – Timing	1.3			µs
t_{set}	SMBus SDA setup time from SCL		100			ns
t_{hold}	SMBus SDA hold time from SCL		300			ns
	SMBus START/STOP condition setup/hold time from SCL		600			ns
T_{low}	SCL low period		1.3			µs
T_{high}	SCL high period		0.6			µs

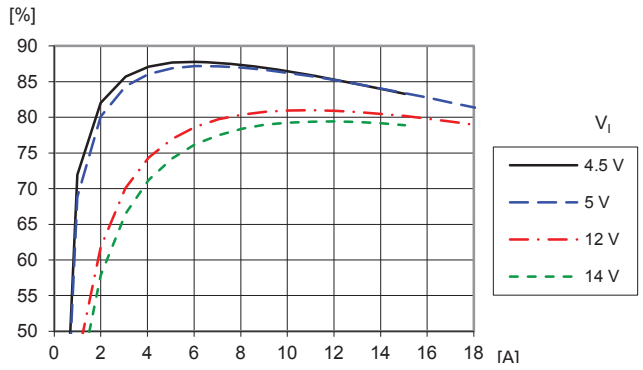
Characteristics		Conditions	Min	Typ	Max	Unit
Initialization time		From $V_I > V_{UVLO}$ to ready to be enabled		23		ms
Soft-start On Delay Time Note 5	Delay duration			10		ms
	Delay duration range	PMBus configurable TON_DELAY		1-145		ms
	Delay set resolution			0.6		ms
	Delay set accuracy	TON_DELAY value sent versus read-back		±0.5 x Delay set resolution		ms
	Delay accuracy	Actual delay duration versus TON_DELAY read-back		±0.8		ms
Soft-start Rise Time (0-100% of V_0) Note 5	Ramp duration			10		ms
	Ramp duration range	PMBus configurable TON_RISE		1 - (255 x Ramp set resolution)		ms
	Ramp set resolution	Varies with V_0	0.4		1	ms
	Ramp set accuracy	TON_RISE value sent versus read-back		±0.5 x Ramp set resolution		ms
	Ramp time accuracy	Actual ramp duration versus TON_RISE read-back		±10		µs
Compensation Calibration	Signal duration			5		ms
	Signal level	V_0 = 0.6 V		3.5		% V_0
		V_0 = 1.2 – 1.8 V		2.5		% V_0
Power Good , PG	PG threshold	Rising		90		% V_0
		Falling		85		% V_0
		Tracking mode See section Voltage Tracking		450		mV
	PG thresholds range (Non-tracking only)	PMBus configurable POWER_GOOD_ON POWER_GOOD_OFF	0		100	% V_0
	PG delay Enabled compensation calibration (default)	From V_0 reaching target to PG assertion		11		ms
		Tracking mode See section Voltage Tracking		20		ms
	PG delay Disabled compensation calibration	From V_0 reaching PG rising threshold to PG assertion		0		ms
		Tracking mode See section Voltage Tracking		20		ms
Tracking Input Voltage Range		CS_VTRK pin Note 6	0		1.2	V
Tracking Accuracy			-100		100	mV
Monitoring accuracy	Input voltage READ_VIN			±3		% V_I
	Output voltage READ_VOUT			±1		% V_0
	Output current READ_IOUT Note 7	TP_1 = 0-95°C, V_I = 4.5-14 V, I_0 > 5 A		±8.5		% I_0
		TP_1 = 0-95°C, V_I = 4.5-14 V, I_0 < 5 A		±0.4		A
	Temperature READ_ TEMPERATURE_1	Note 4	-5		5	°C
	Duty cycle READ_DUTY_CYCLE	Duty cycle < 10%	-3		3	%
		Duty cycle > 10%	-1	±0.5	1	%

Note 1. Value refers to total (internal + external) effective output capacitance. Capacitance derating with VO typical for ceramic capacitors (bias characteristics) and temperature variations must be considered for the external capacitor(s). See section External Output Capacitors.
Note 2. A switching frequency close to 475 kHz should not be used since this frequency represents a boundary of two operational modes of the product. There are configuration changes to consider when changing the switching frequency, see section Switching Frequency.
Note 3.The restart interval is configurable between 100ms and 700ms in 100ms steps. Severe overcurrent faults occurring with VO > 2.5V may result in a restart interval of 1200 ms instead of the configured value. See operating conditions for other fault response alternatives.
Note 4. Temperature measured internally at temperature position P3. See section Over Temperature Protection.
Note 5. Same specification applies for soft-stop and TOFF_DELAY/TOFF_FALL if enabled. The internal ramp and delay generators can only achieve certain discrete timing values. A written TON/OFF_DELAY or TON/OFF_RISE value will be rounded to the closest achievable value, thus a command read-back provides the actual set value. See section Soft-Start and Soft-Stop.
Note 6.Larger tracking input range is provided by external resistor divider, see section Voltage Tracking.
Note 7. At VO > 3.5V and VO / VI in the approximate range 55-70% there may be an additional current monitoring inaccuracy on the negative side up to -1 A.

Typical Characteristics, V_O = 0.6 V

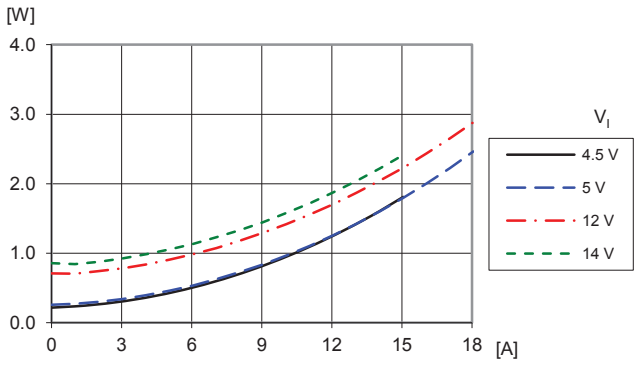
Default Configuration, T_{P1} = +25°C

Efficiency



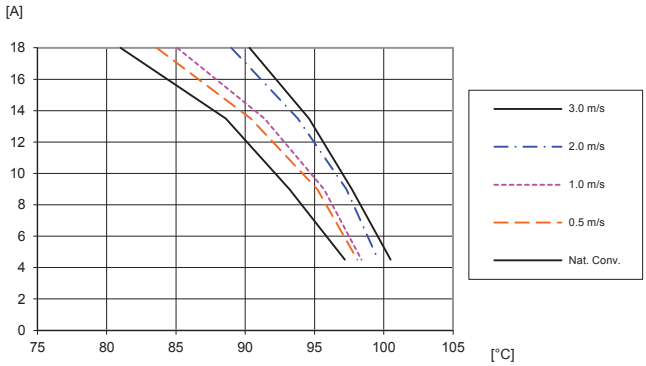
Efficiency vs. load current and input voltage.

Power Dissipation



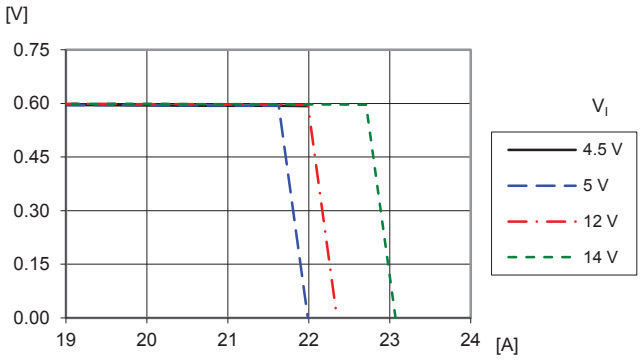
Dissipated power vs. load current and input voltage.

Output Current Derating



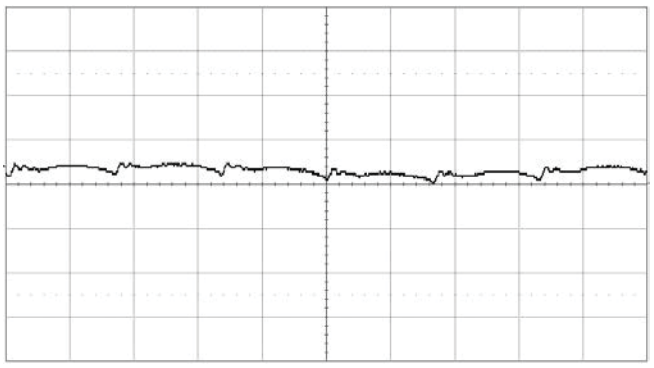
Available load current vs. ambient air temperature and airflow at V_I = 12 V. See section Thermal Consideration.

Current Limit Characteristics



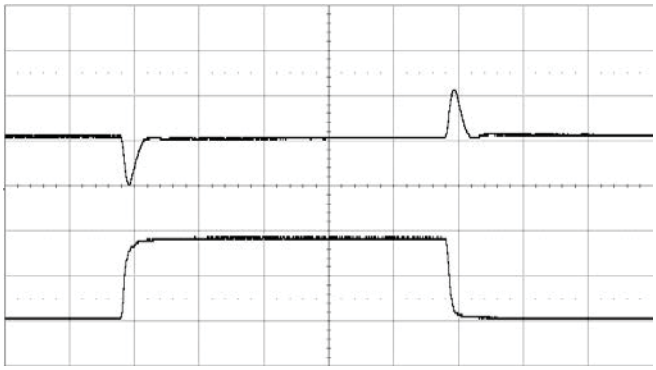
Output voltage vs. load current and input voltage.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, C_O = 3x100 µF, I_O = 18 A.
Scale: 5 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

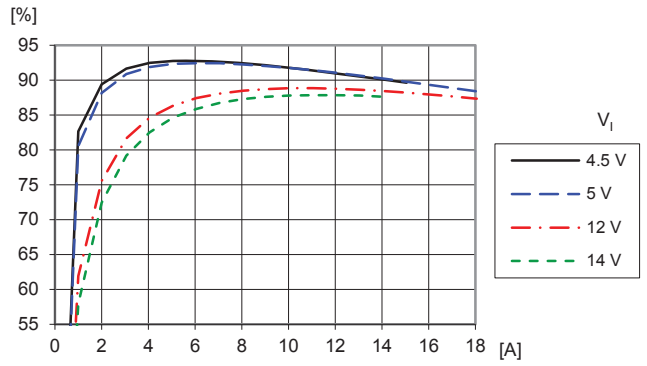


Output voltage response to load current step change (4.5–13.5–4.5 A) at V_I = 12 V, C_O = 3x100 µF + 270 µF/10mΩ. Default compensation settings.
Scale: 50 mV/div, 5 A/div, 100 µs/div.

Typical Characteristics, V_O = 1.2 V

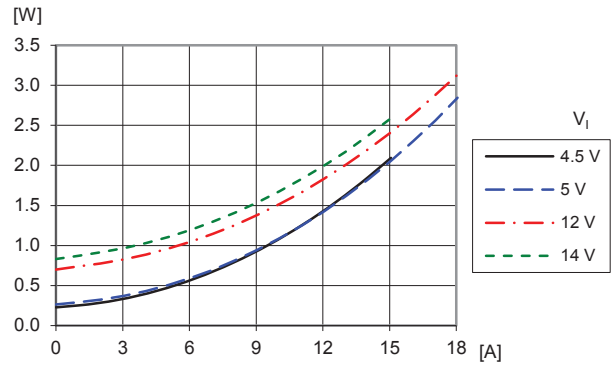
Default Configuration, T_{P1} = +25°C

Efficiency



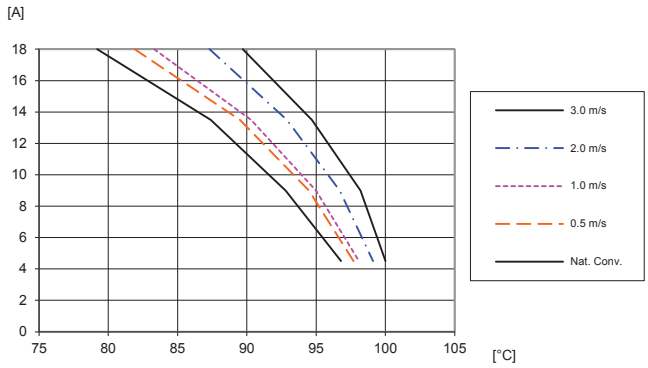
Efficiency vs. load current and input voltage.

Power Dissipation



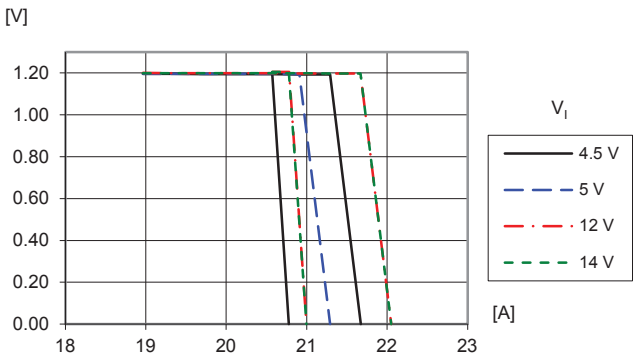
Dissipated power vs. load current and input voltage.

Output Current Derating



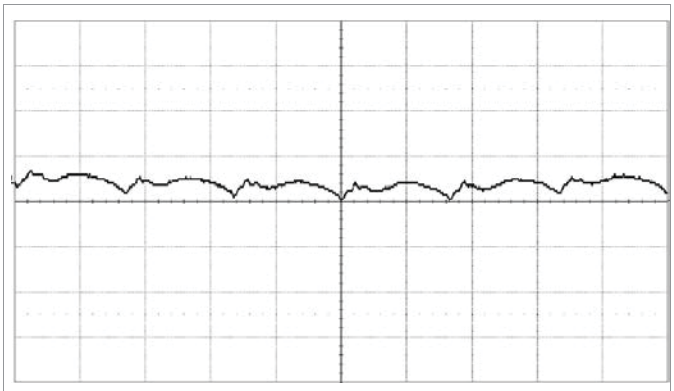
Available load current vs. ambient air temperature and airflow at V_I = 12 V. See section Thermal Consideration.

Current Limit Characteristics



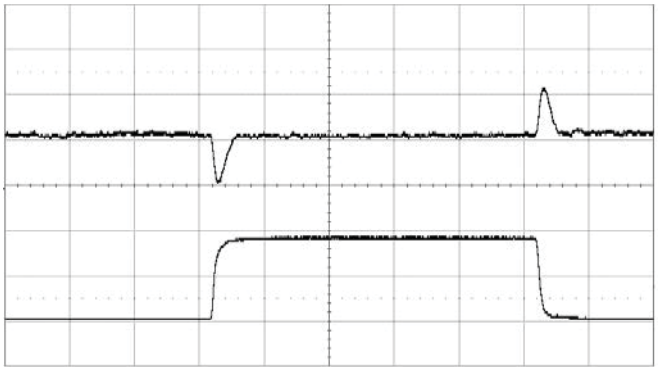
Output voltage vs. load current and input voltage.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, C_O = 3x100 µF, I_O = 18A.
Scale: 5 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

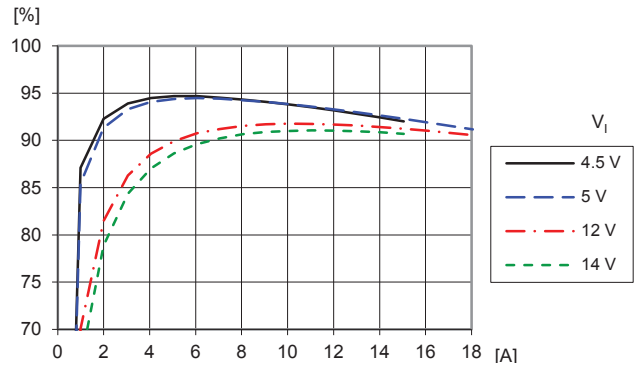


Output voltage response to load current step change (4.5–13.5–4.5 A) at V_I = 12 V, C_O = 3x100 µF + 270 µF/10mΩ. Default compensation settings.
Scale: 50 mV/div, 5 A/div, 100 µs/div.

Typical Characteristics, V_O = 1.8 V

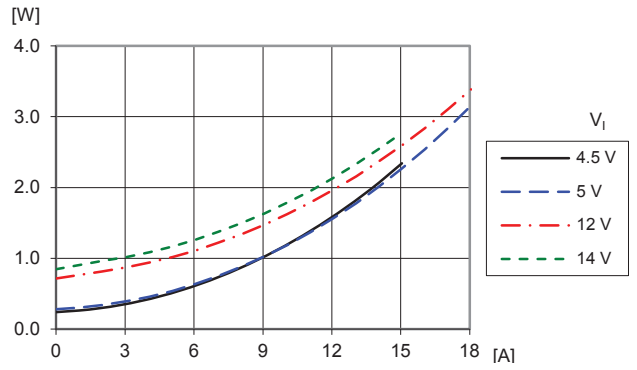
Default Configuration, T_{P1} = +25°C

Efficiency



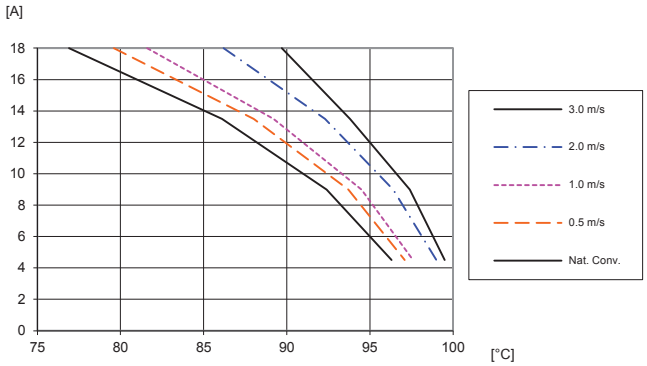
Efficiency vs. load current and input voltage.

Power Dissipation



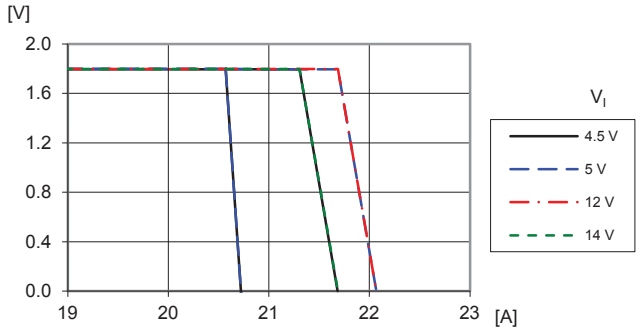
Dissipated power vs. load current and input voltage.

Output Current Derating



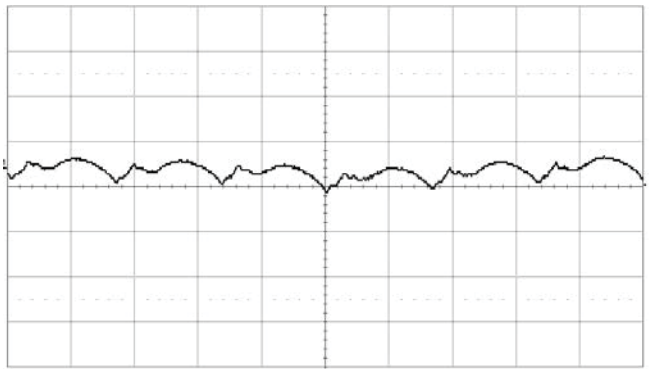
Available load current vs. ambient air temperature and airflow at V_I = 12 V. See section Thermal Consideration.

Current Limit Characteristics



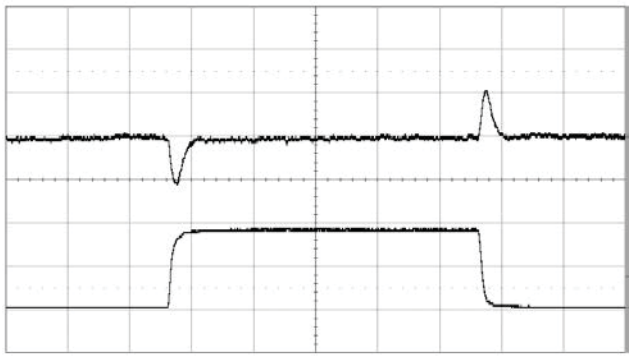
Output voltage vs. load current and input voltage.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, C_O = 3x100 µF, I_O =18 A.
Scale: 5 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

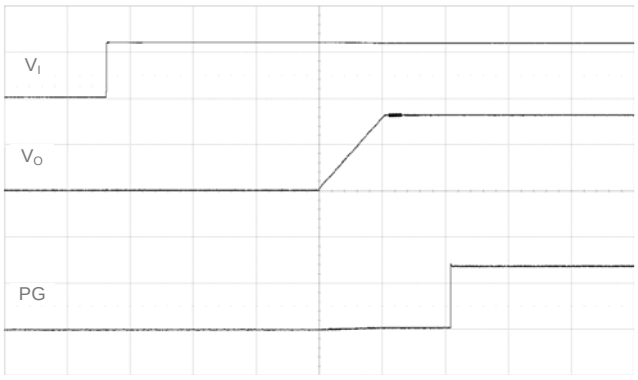


Output voltage response to load current step change (4.5–13.5–4.5 A) at V_I = 12 V, C_O = 3x100 µF + 270 µF/10mΩ. Default compensation settings.
Scale: 50 mV/div, 5 A/div, 100 µs/div.

Typical Characteristics

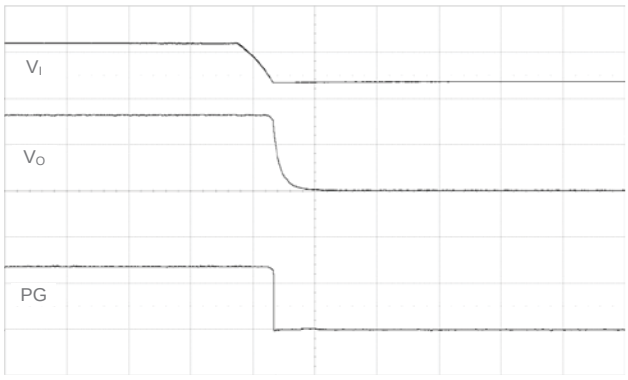
Default Configuration, T_{P1} = +25°C, V_O = 1.8 V

Start-up by input source



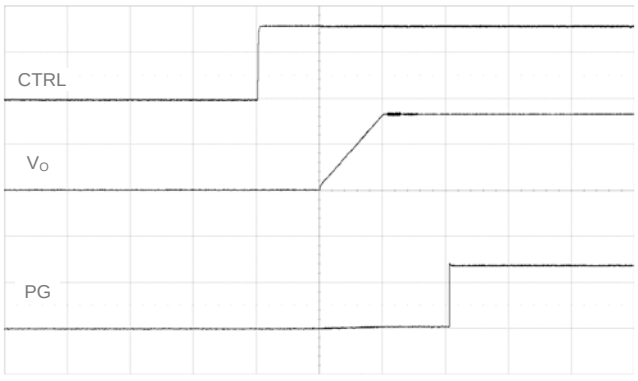
Start-up enabled by applying V_I. TON_DELAY = TON_RISE = 10 ms (default).
V_I = 12 V, I_O = max I_O, PG pulled up to V_O.
Scale: 10 or 1 V/div, 10 ms/div.

Shut-down by input source



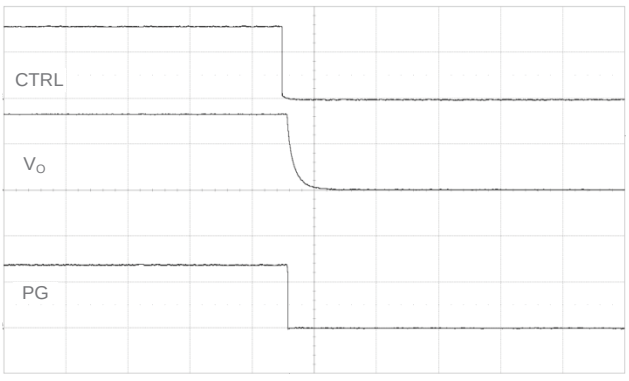
Shut-down by removing V_I.
V_I = 12 V, I_O = max I_O, PG pulled up to V_O.
Scale: 10 or 1 V/div, 1 ms/div.

Start-up by CTRL signal



Start-up enabled by CTRL signal. TON_DELAY = TON_RISE = 10 ms (default).
V_I = 12 V, I_O = max I_O, PG pulled up to V_O.
Scale: 2 or 1 V/div, 10 ms/div.

Shutdown by CTRL signal

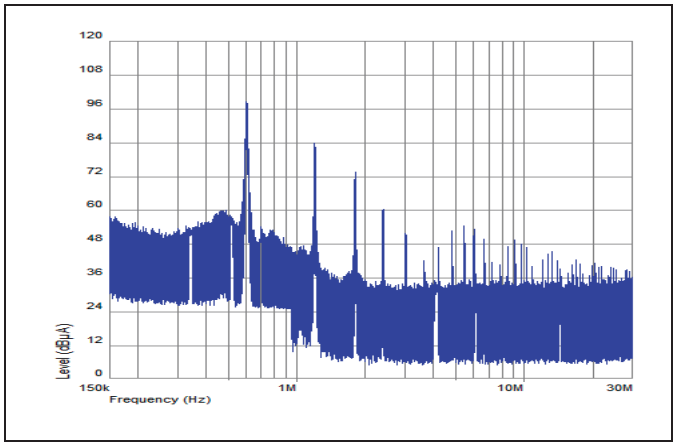


Shut-down by CTRL signal.
V_I = 12 V, I_O = max I_O, PG pulled up to V_O.
Scale: 2 or 1 V/div, 1 ms/div.

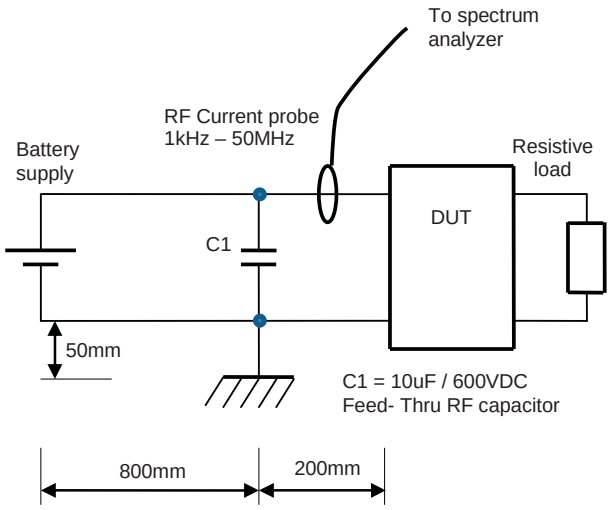
EMC Specification

Conducted EMI is measured according to the test set-up below. The fundamental switching frequency is 600 kHz.

Conducted EMI Input terminal value (typical for default configuration)



EMI without filter



Test set-up conducted emission, power lead

Layout Recommendations

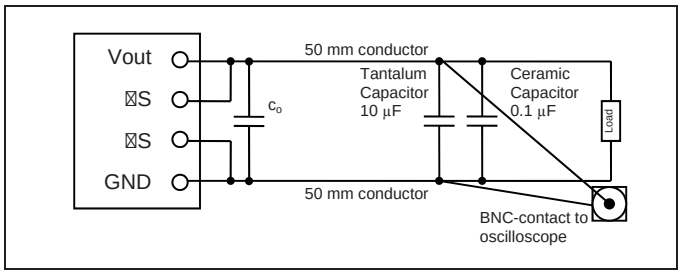
The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output Ripple and Noise

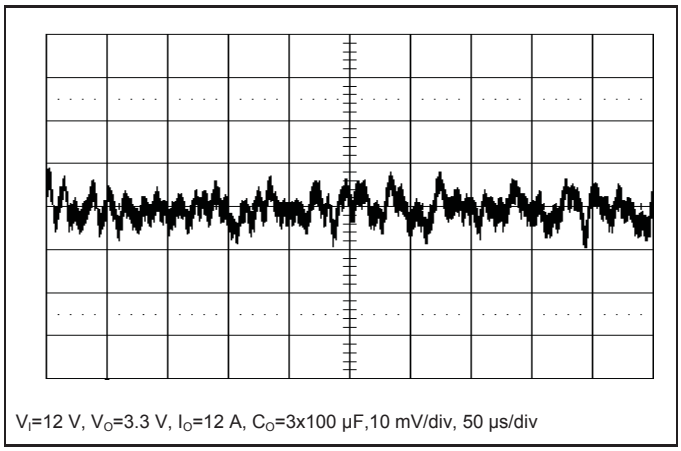
Output ripple and noise is measured according to figure below.

A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up

The digital compensation of the product is designed to automatically provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low-frequency noise or wander at the output, in addition to the fundamental switching frequency output ripple. The total output ripple and noise is maintained at a low level.



Example of low frequency noise at the output

Operating information

Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement
with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin.
The product is delivered with a default configuration suitable for a wide range of operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Please contact your local Murata Power Solutions representative for design support of custom configurations or appropriate SW tools for design and download of your own configurations.

Input Under Voltage Lockout, UVLO

The product provides a non-configurable under voltage lockout (UVLO) circuit that monitors the internal supply of the converter. Below a certain input voltage level the internal supply will be too low for proper operation and the product will be in under voltage lockout, not switching or responding to the CTRL pin or to PMBus commands.

Input Over Voltage Lockout, OVLO

The product provides a non-configurable over voltage lockout (OVLO) circuit that will shut down the product when the input voltage rises above a certain level. The product will not switch, respond to the CTRL pin or to PMBus commands when being in over voltage lockout.

Input Turn-On and Turn-Off Voltage

The product monitors the input voltage and will turn-on and turn-off the output at configured levels (assuming the product is enabled by CTRL pin or PMBus). The default turn-on input voltage level is 4.35 V whereas the corresponding turn-off input voltage level is 3.8 V. The turn-on and turn-off levels may be reconfigured using the PMBus commands VIN_ON and VIN_OFF.

Input Under Voltage Protection (IUVP)

The product monitors the input voltage continously and will respond as configured when the input voltage falls below the configured threshold level. The product can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by an output voltage shutdown if the fault still exists.
3. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus or the output voltage is re-enabled.
4. Immediate shutdown of output voltage while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

The default response is 4. The IUVP function can be reconfigured using the PMBus commands VIN_UV_FAULT_LIMIT and VIN_UV_FAULT_RESPONSE.

Input Over Voltage Protection (IOVP)

The product monitors the input voltage continously and will respond as configured when the input voltage rises above the configured threshold level. Refer to section “Input Under Voltage Protection” for response configuration options and default setting.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

The input ripple RMS current in a buck converter can be estimated to Eq. 1. $I_{inputRMS} = I_{load}\sqrt{D(1-D)}$,
where I_{load} is the output load current and D is the duty cycle. The maximum load ripple current becomes $I_{load}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

It is recommended to use at least 47 uF of ceramic input capacitance. At duty cycles between 25% and 75% where the input ripple current increases (see Eq. 1), additional ceramic capacitance will help to keep the input ripple voltage low. The required bulk capacitance depends on the impedance of the input source and the load transient levels at the output. In general a low-ESR bulk capacitor of at least 100 uF is recommended. The larger the duty cycle is, the larger impact an output load step will have on the input side, thus the larger bulk capacitance is required to limit the input voltage deviation.

If several products are connected in a phase spreading setup the amount of input capacitance per product can be reduced.

Input Capacitors must be placed closely and with low impedance connections to the VIN and GND pins in order to be effective.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low

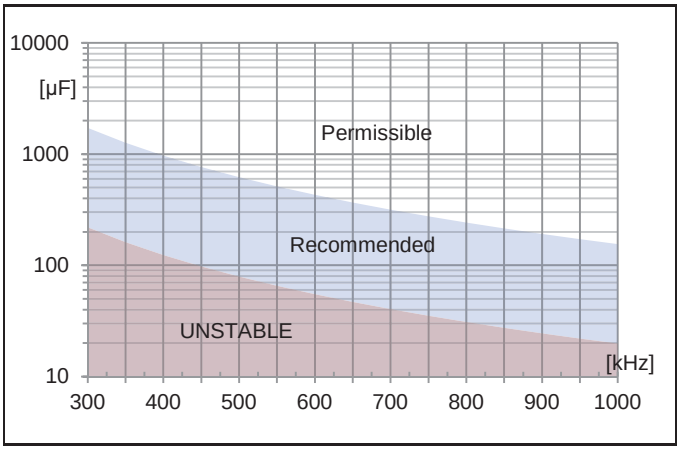
ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A small output voltage deviation during load transients is achieved by using a larger amount of capacitance. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to achieve a small output deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product (see section Compensation Implementation).

It is recommended to locate low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts and cabling in order for capacitance to be effective.

The control loop of the product is optimized to operate with low-ESR output capacitors and is capable of achieving a fast loop transient response with a reduced amount of capacitance. The effective output capacitance is recommended to be in the range [COUT_low, COUT_high] according to equations Eq. 2 and Eq. 3 below, where FSW is the switching frequency. The compensation implementation of the product is optimized for this range.

Eq. 2. $$C_{OUT\_low} = \frac{2.6 \cdot 10^7}{(F_{SW})^2}$$

Eq. 3. $$C_{OUT\_high} = \frac{16 \cdot 10^7}{(F_{SW})^2}$$



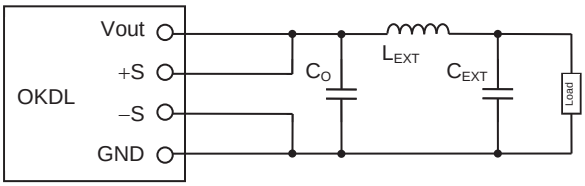
Effective total output capacitance limits vs switching frequency.

The product permits a large range of output capacitance, thus capacitance above COUT_high is acceptable. This capability is important in applications where the output capacitance may be unknown or not well controlled or in applications where a large amount of output capacitance is required. The limit of COUT_low must be followed in order to guarantee stability.

Note that Eq. 2 and Eq. 3 and the chart above refer to the total capacitance at the output, thus including both the capacitance internal to the product and the external capacitance applied in the application. The internal output capacitance is listed in the Electrical Characteristics table.

Note also that Eq. 2 and Eq. 3 and the chart refers to the effective capacitance, not taking into account the capacitance derating that applies for ceramic capacitors with increased voltage or temperature variations.

In cases where the external output filter includes an inductor (forming a pi filter) according to the picture below, the following must be considered.



External output filter with inductor (pi filter).

In order for the compensation calibration (see next sections) to give a reliable result, the following condition should be fulfilled:

$$F_{LC\_EXT} = \frac{1}{2\pi\sqrt{L_{EXT}\, C_{EXT}}} > \frac{F_{SW}}{10}$$

where FLC_EXT is the resonance frequency of the external filter and FSW is the switching frequency. If there are multiple pi filters in parallel on the output, giving a more complex transfer function with several resonance peaks, each of the peaks should be above FSW/10.

If this condition is not fulfilled it is recommended to disable compensation calibration and set FLC manually in COMP_MODEL (see next sections). Please contact your Murata Power Solutions sales representative for further support.

For the OKDL products, it is recommended that the remote sense connections are made at a point before the external inductor, as illustrated in the drawing above.

Dynamic Loop Compensation (DLC)

The typical design of regulated power converters includes a control function with a feedback loop that can be closed using either analog or digital circuits. The feedback loop is required to provide a stable output voltage, but should be optimized for the output filter to maintain output voltage regulation during transient conditions such as sudden changes in output current and/or input voltage. Digitally controlled converters allow one to optimize loop parameters without the need to change components on the board, however, optimization

can still be challenging because the key parameters of the output filter include parasitic impedances in the PCB and the often distributed filter components themselves.

Dynamic Loop Compensation has been developed to solve the problem of compensation for a converter with a difficult to define output filter. This task is achieved by utilization of algorithms that can characterize an arbitrary output filter based on behavior of the output voltage in response to a disturbance initiated by the algorithm, or occurring due to the changes in operating conditions, and automatically adjust feedback loop parameters to match the output filter.

Details of the algorithm that is used to characterize an output filter and the different operational modes can be found in the following sections.

Compensation Implementation

Unlike PID-based digital power regulators the product uses a state-space model based algorithm that is valid for both the small- and large-signal response and accounts for duty-cycle saturation effects. This eliminates the need for users to determine and set thresholds for transitioning from linear to nonlinear modes. These capabilities result in fast loop transient response and the possibility of reducing the number of output capacitors.

Compensation calibration is when the resonance frequency FLC of the output stage is measured. The FLC value is used to automatically control the compensation. During ramp-up of the output voltage, robust and low bandwidth default compensation settings are used based on the default FLC value assigned by bits 15:0 in PMBus command COMP_MODEL. If the switching frequency is changed the default FLC should be adjusted according to Eq. 4 to maintain robust settings.

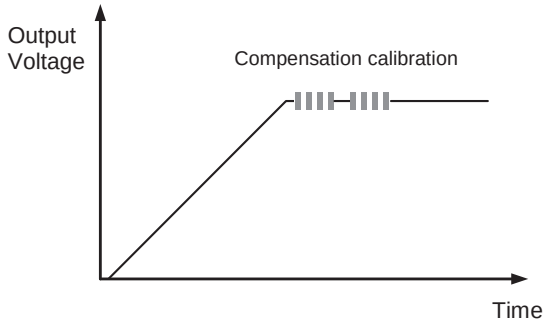
Eq. 4. $$F_{LC\_DEFAULT} = \frac{F_{SW}}{32}$$

It is possible for the user to write any FLC value in COMP_MODEL to be used during ramp-up. This is useful in cases where improved dynamic performance is needed during ramp-up. User assignment of FLC in COMP_MODEL is also needed when calibration is disabled, since in such case the FLC value used during ramp-up will continue to be used when ramp-up has finished.

When calibration is enabled (default), an AC low amplitude measurement signal is applied on the output immediately after ramp-up has finished. See Electrical Characteristics table for a specification of this measurement signal. During calibration the resonant frequency FLC of the power stage is measured. From the result an internal nonlinear model is constructed to optimize the bandwidth and transient response of the product. Pole locations of the closed system are automatically selected based on switching frequency, measured FLC and the output voltage level.

After each performed calibration, bits 15:0 in COMP_MODEL are updated with measured FLC, thus this value can be read out by the user. Note however, as soon as the output voltage is disabled, the FLC value in COMP_MODEL will revert back to the corresponding value stored in User NVM. Therefore, user values of COMP_MODEL should be written to NVM, or, if written to RAM only, be written before each time the output voltage is enabled. COMP_MODEL should only be changed in RAM while the output voltage is disabled.

By setting bit 2 in ADAPTIVE_MODE a STORE_USER_ALL command will automatically be performed after the next calibration, effectively storing the measured FLC value in COMP_MODEL 15:0 in NVM as the FLC value for subsequent ramp-ups.



The table below shows an example of improvement in transient response due to the compensation calibration, compared to using the FLC_DEFAULT value.

	Non-calibrated compensation	Calibrated compensation
Voltage deviation	53 mV	34 mV
Recovery time	50 µs	30 µs

Load transient performance non-calibrated compensation with FLC_DEFAULT vs. calibrated compensation.
VI=12 V, VO=1.2 V, CO = 3x100 µF + 270µF/10mΩ, load step 3-9-3 A, 1 A/us.

The PMBus command ADAPTIVE_MODE provides the user different options for compensation calibration:

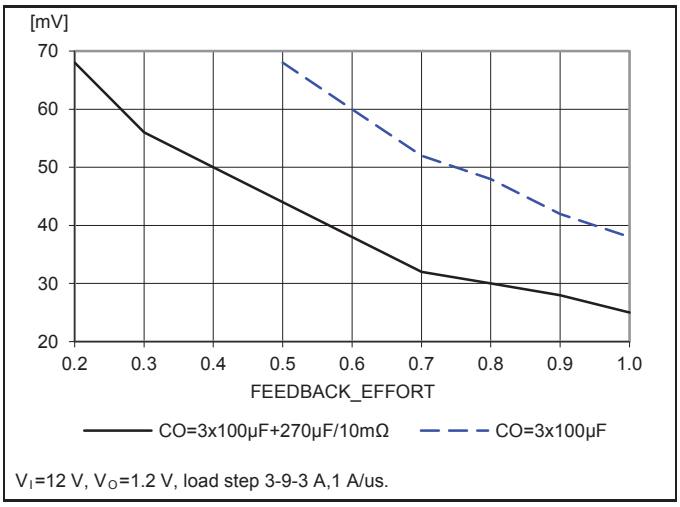
1. Calibration is performed once after each ramp-up (default). (ADAPTIVE_MODE = 0x024B).
2. Calibration is performed once after first ramp-up after input voltage is applied (ADAPTIVE_MODE = 0x124B).
3. Calibration is performed continuously after ramp-up at ~800 ms interval (ADAPTIVE_MODE = 0x034B).
4. Calibration is disabled (ADAPTIVE_MODE = 0x004B). The FLC value stored in bits 15:0 in COMP_MODEL will be applied.
5. Calibration is performed continuously in response to a PMBus command. Controlled by setting/clearing bit 8 in ADAPTIVE_MODE during operation.

Compensation may be set more or less aggressive by adjusting the feedback gain factor, controlled by the PMBus command FEEDBACK_EFFORT. This parameter is proportional to the open loop gain of the system. Increasing the gain, i.e the control effort, will reduce the voltage deviation at load transients, at the expense of somewhat increased jitter and noise on the output. Users also have access to

the PMBus command ZETAP, which corresponds to the damping ratio of the closed loop system. By default the product uses 0.5 as the feedback gain factor and 1.5 for damping ratio, to target a system bandwidth of 10% of the switching frequency.

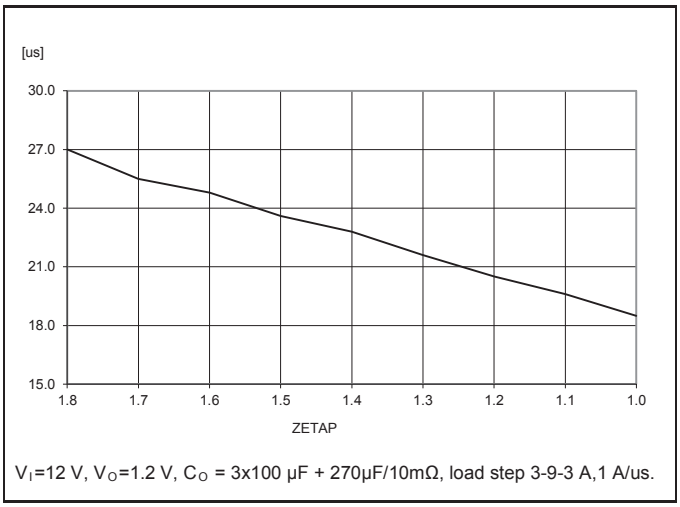
In some operating conditions at low output voltages, it is possible to enhance the recovery time at load release by enabling Negative Duty Cycle by PMBus command LOOP_CONFIG.

The graphs below exemplify the impact on load transient performance when adjusting the feedback gain factor, the damping ratio and the Negative Duty Cycle feature.



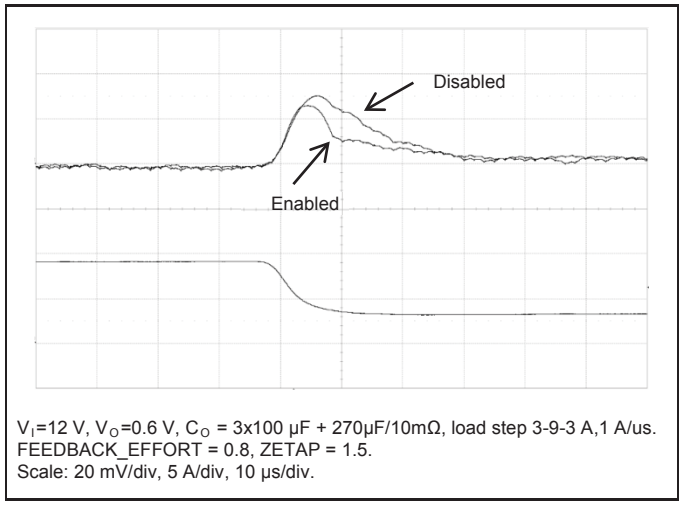
V_I=12 V, V_O=1.2 V, load step 3-9-3 A,1 A/us.

Voltage deviation vs. FEEDBACK_EFFORT setting.



V_I=12 V, V_O=1.2 V, C_O = 3x100 µF + 270µF/10mΩ, load step 3-9-3 A,1 A/us.

Recovery time to within 1% of VO vs. ZETAP setting.



V_I=12 V, V_O=0.6 V, C_O = 3x100 µF + 270µF/10mΩ, load step 3-9-3 A,1 A/us.
FEEDBACK_EFFORT = 0.8, ZETAP = 1.5.
Scale: 20 mV/div, 5 A/div, 10 µs/div.

Load release response at enabled/disabled Negative Duty Cycle at low output voltage.

Remote Sense

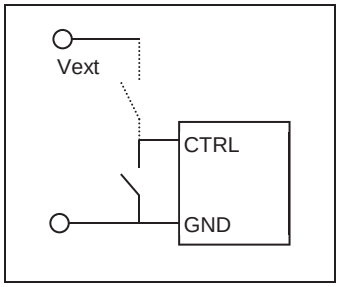
The product has remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PWB ground layer to reduce noise susceptibility. Due to derating of internal output capacitance the voltage drop should be kept below VDROPMAX = (5.25 – VOUT) / 2. A large voltage drop will impact the electrical performance of the regulator. If the remote sense is not needed +S must be connected to VOUT and –S must be connected to GND.

Output Voltage Control

To control the output voltage the product features both a remote control input through the CTRL pin and a PMBus enable function by the command OPERATION. It is also possible to configure the output to be always on.

By default the output is controlled by the CTRL pin only. The output voltage control can be reconfigured using the PMBus command ON_OFF_CONFIG.

Remote Control



The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to either the primary negative input connection (GND) or an external voltage (Vext). See Absolute Maximum Rating for maximum voltage level allowed at the CTRL pin.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch.

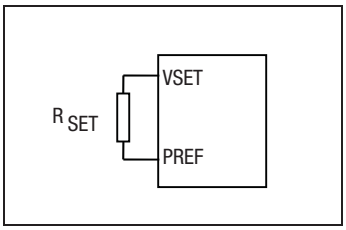
The CTRL pin has an internal 6.8 kΩ pull-up resistor to 3.3 V. The external device must provide a minimum required sink current to guarantee a voltage not higher than the logic low threshold level (see

Electrical Characteristics). When the CTRL pin is left open, the voltage generated on the CTRL pin is 3.3 V.

By default the product provides "positive logic" RC and will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. It is possible to configure "negative logic" instead by using the PMBus command ON_OFF_CONFIG.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the CTRL pin.

Output Voltage Adjust using Pin-strap Resistor



Using an external Pin-strap resistor, RSET, the output voltage can be set in the range 0.6 V to 5.0 V at 16 different levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin.

RSET also sets the maximum output voltage; see section "Output Voltage Range Limitation". The resistor is sensed only at the application of input voltage. Changing the resistor value during normal operation will not change the output voltage. The input voltage must be at least 1 V larger than the output voltage in order to deliver the correct output voltage. See Ordering Information for output voltage range.

The following table shows recommended resistor values for RSET. Maximum 1% tolerance resistors are required.

V_{OUT} [V]	R_{SET}[kΩ]	V_{OUT} [V]	R_{SET}[kΩ]
0.60	5.11	1.05	17.8
0.70	6.19	1.10	21.5
0.75	7.15	1.20	26.1
0.80	8.25	1.50	31.6
0.85	9.53	1.80	38.3
0.90	11.0	2.50	44.2
0.95	12.7	3.30	51.1
1.00	14.7	5.00	59.0

Output Voltage Adjust using PMBus

The output voltage set by pin-strap can be overridden using the PMBus command VOUT_COMMAND. See Electrical Specification for adjustment range.

Voltage Margining Up/Down

Using the PMBus interface it is possible to adjust the output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW, VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION.

Output Voltage Trim

The actual output voltage can be trimmed to optimize performance of a specific load by setting a non-zero value for PMBus command VOUT_TRIM. The value of VOUT_TRIM is summed with VOUT_COMMAND, allowing for multiple products to be commanded to a common nominal value, but with slight adjustments per load.

Output Voltage Range Limitation

The output voltage is by default limited to the least of 5.5 V or 110% of the nominal output voltage, where the nominal output voltage is defined by pin-strap or by VOUT_COMMAND in Non-Volatile Memory (see section Initialization Procedure). This protects the load from an over voltage due to an accidentally written wrong VOUT_COMMAND. The limitation applies to the regulated output voltage, rather than the internal value of VOUT_COMMAND. The output voltage limit can be reconfigured using the PMBus command VOUT_MAX.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. The product can be configured to respond in different ways to the output voltage exceeding the OVP limit:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by an output voltage shutdown if the fault still exists.
3. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus or the output voltage is re-enabled.
4. Immediate shutdown of output voltage while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

The default response is 4. The OVP limit and fault response can be reconfigured using the PMBus commands VOUT_OV_FAULT_LIMIT and VOUT_OV_FAULT_RESPONSE.

Output Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. Refer to section "Output Over Voltage Protection" for response configuration options and default setting.

Power Good

PG (Power Good) is an active high open drain output used to indicate when the product is ready to provide regulated output voltage to the load. During startup and during a fault condition, PG is held low.

By default, PG is asserted high after the output has ramped to a voltage above 90% of the nominal voltage and a successful compensation calibration has completed.

By default, PG is deasserted if the output voltage falls below 85% of the nominal voltage. These limits may be changed using the PMBus commands POWER_GOOD_ON and POWER_GOOD_OFF.

The PG output is not defined during ramp up of the input voltage due to the initialization of the product.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at continuous overload. After ramp-up is complete the product can detect an output overload/short condition. The following OCP response options are available:

1. Continue operating without interruption (this could result in permanent damage to the product).
2. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus or the output voltage is re-enabled.
3. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response from an over current fault is 3. Note that delayed shutdown is not supported. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response can be reconfigured using the PMBus commands IOUT_OC_FAULT_LIMIT and IOUT_OC_FAULT_RESPONSE.

If option 2 above is to be used, the TON_MAX_FAULT_RESPONSE setting should match the setting of IOUT_OC_FAULT_RESPONSE in order to make sure that no restart attempts occur.

Switching Frequency

The default switching frequency yields optimal performance. The switching frequency can be re-configured in a certain range using the PMBus command FREQUENCY_SWITCH. Refer to Electrical Specification for default switching frequency and range.

If changing the switching frequency more than +/-10% from the default value, the following should be considered to maintain reliable operation:

- The default FLC value in COMP_MODEL should be adjusted, see section Compensation Implementation.
- Adjustment of the fixedDTR and fixedDTF values in DEADTIME_GCTRL may be required, for higher switching frequencies in particular.

Changing the switching frequency will affect efficiency/power dissipation, load transient response and output ripple.

Synchronization

The product may be synchronized with an external clock to eliminate beat noise on the input and output voltage lines by connecting the clock source to the SYNC pin. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The clock frequency of the external clock source must be stable prior to enabling the output voltage. Further, the PMBus command FREQUENCY_SWITCH must be set to a value close to the frequency of the external clock prior to enabling the output voltage, in order to set the internal controller in proper operational mode.

The product automatically checks for a clock signal on the SYNC pin when input power is applied and when the output is enabled. If no incoming clock signal is present, the product will use the internal oscillator at the configued switching frequency.

In the event of a loss of the external clock signal during normal operation, the product will automatically switch to the internal oscillator and switch at a frequency close to the original SYNC input frequency.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized.

The phase offset is measured from the rising edge of the applied external clock to the center of the PWM pulse as illustrated below.

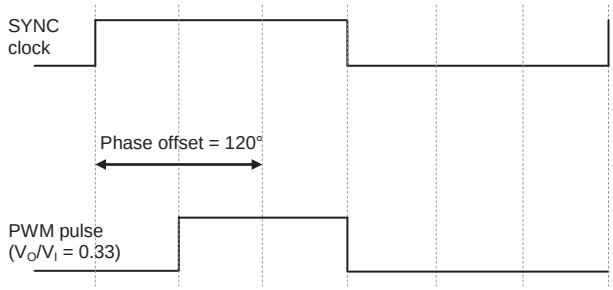


Illustration of phase offset.

By default the phase offset is controlled by the defined PMBus address (see section PMBus Interface) according to the table below. This provides a way to configure phase spreading with up to eight different phase positions without using a PMBus command.

Set PMBus address	Phase offset
xxxx000b	0°
xxxx001b	60°
xxxx010b	120°
xxxx011b	180°
xxxx100b	240°
xxxx101b	300°
xxxx110b	90°
xxxx111b	270°

The default phase offset can be overridden by using the standard PMBus command INTERLEAVE. The phase offset can then be defined as

$$Phase\_offset(°) = 360° \times \frac{Interleave\_order}{Number\ in\_group}$$

Interleave_order is in the range 0-15. Number_in_group is in the range 0-15 where a value of 0 means 16. The set resolution for the phase offset is 360° / 128 ≈ 2.8°.

Giving the PMBus command INTERLEAVE a value of 0x0000 will revert back to the default address controlled phase offset.

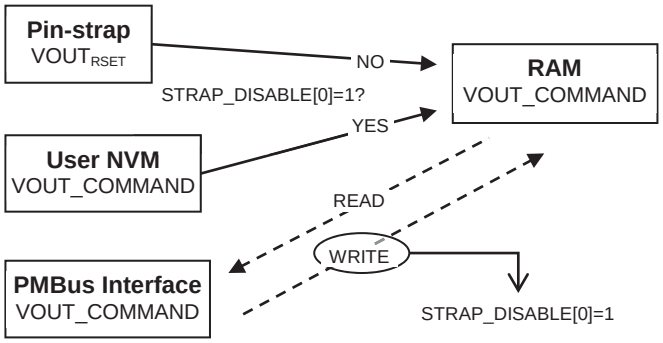
Murata Power Solutions provides software tools for convenient configuration of optimized phase spreading, allowing the amount of input capacitance to be significantly reduced.

Initialization Procedure

The product follows an internal initialization procedure after power is applied to the VIN pin (refer to figure below):

1. Self test and memory check.
2. The address pin-strap resistors are measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured. The associated output voltage level will be loaded into operational RAM memory, unless an overriding PMBus command VOUT_COMMAND has been explicitly written and stored in the User Non-Volatile Memory (indicated by bit 0 in command STRAP_DISABLE).
4. Values stored in the User Non-Volatile Memory (NVM) are loaded into operational RAM memory. For PMBus commands listed in the table below, loaded values will be based on the output voltage level loaded in step 3 above, unless the commands have been explicitly written and stored in the User NVM.
5. Check for external clock signal at the SYNC pin and wait for lock if used.

Once this procedure is completed and the initialization time has passed (see Electrical Specification), the output voltage is ready to be enabled and the PMBus interface can be used.



Loading of nominal output voltage level

Note the following implications of the initialization procedure:

- If the RSET pin-strap resistance is changed, input voltage will have to be cycled before the output voltage level is affected.
- If VOUT_COMMAND is changed and stored to User NVM, input voltage will have to be cycled before the output voltage related commands in the table below are re-scaled according to the new output voltage level.

See section PMBus Interface for more information about the Non-Volatile Memories (NVM) of the product.

Soft-start and Soft-stop

Vout related PMBus command	Loaded value unless explicitly written + stored to User NVM.
POWER_GOOD_ON	0.90 x loaded Vout level
POWER_GOOD_OFF	0.85 x loaded Vout level
VOUT_MAX	1.10 x loaded Vout level
VOUT_MARGIN_HIGH	1.05 x loaded Vout level
VOUT_MARGIN_LOW	0.95 x loaded Vout level
VOUT_OV_FAULT_LIMIT	1.15 x loaded Vout level
VOUT_UV_FAULT_LIMIT	0.85 x loaded Vout level

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.

The rise time is the time taken for the output to ramp to its target voltage while the fall time is the time taken for the output to ramp down from its regulation voltage to less than 10% of that value. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The off delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

Soft-stop is disabled by default but may be enabled through the

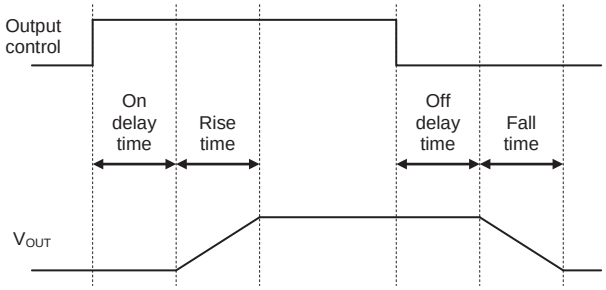


Illustration of Soft-Start and Soft-Stop

PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

The internal delay generator can only achieve certain discrete timing values. A written TON_DELAY/TOFF_DELAY value will be rounded to the closest achievable value, thus a TON_DELAY/OFF_DELAY read will provide the actual set value.

The internal ramp generator can only achieve certain discrete timing values for a given combination of switch frequency, output voltage level, set ramp time and trim data. These values are close, but not

exactly the same, when any of the relevant parameters are altered. A written TON_RISE/TOFF_FALL value will be rounded to the closest achievable value, thus a TON_RISE/TOFF_FALL read will provide the actual set value.

Refer to Electrical Specification for default on delay time and rise time and the configurability ranges and resolutions. The specification provided for soft-start applies also for soft-stop, if enabled.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another. Multi-product sequencing can be achieved by configuring the start delay and rise time of each device through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.

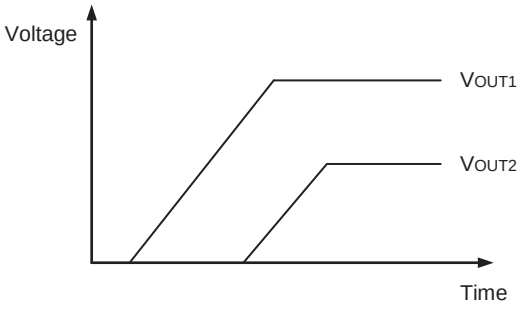


Illustration of Output Voltage Sequencing

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

When the output is enabled the product checks the output for the presence of pre-bias voltage. If the pre-bias voltage is above the output overvoltage threshold the product will not attempt soft-start. If the pre-bias voltage is less than 200 mV the soft-start is performed assuming no pre-bias. If the pre-bias voltage is above 200 mV but below target output voltage, the product ramps up the output voltage from the pre-bias voltage to the target regulation as shown in the figure below.

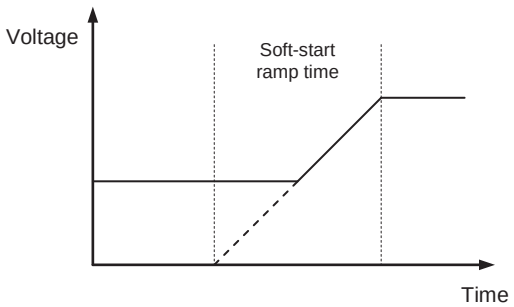
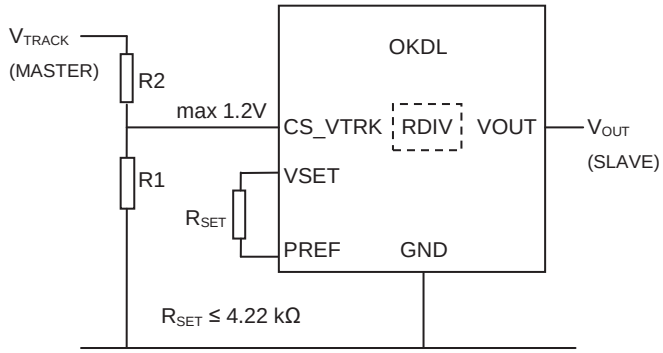


Illustration of Pre-Bias Startup

Voltage Tracking

The product supports tracking of the output from a master voltage applied to the CS_VTRK pin. To select the tracking mode, a resistance ≤ 4.22 kΩ must be connected between the VSET and PREF pins.

The tracking ratio used is controlled by an internal feedback divider RDIV and an external resistive voltage divider (R1, R2) which is placed from the supply being tracked to GND pins.



Tracking Mode Configuration

In tracking mode the output voltage is regulated to the lower of:

Eq. 5 $$V_{OUT} = \frac{V_{TRACK}}{RDIV} \times \frac{R1}{R1 + R2}$$

or the output voltage defined by the PMBus command VOUT_COMMAND.

RDIV is automatically selected based on the value of VOUT_COMMAND as shown in the table below. If VOUT_COMMAND is not defined by the user, it will default to 5.25 V with RDIV= 0.20272.

VOUT_COMMAND [V]	RDIV
< 0.99	0.99547
0.99 to < 1.12	0.88222
1.12 to < 1.28	0.76897
1.28 to < 1.50	0.65572
1.50 to < 1.82	0.54247
1.82 to < 2.29	0.42922
2.29 to < 3.12	0.31597
3.12 to < 5.25	0.20272
VOUT_COMMAND not user defined => 5.25	0.20272

For best tracking accuracy it is recommended that once the product is powered up, the VOUT_COMMAND should not be changed so as to cause a change to the operational RDIV. If such a change in VOUT_COMMAND is required, the user should save the new value to User Non-Volatile Memory (using STORE_USER_ALL command) and recycle the input voltage to set a new RDIV operational value.

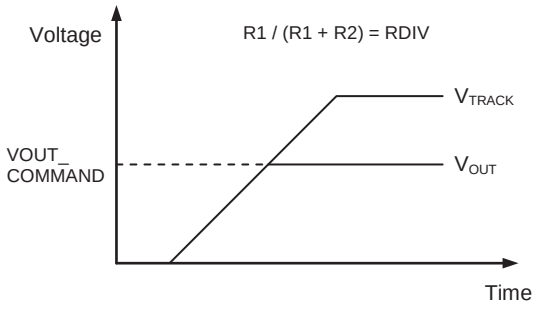
To simplify resistor selection it is recommended to fix R1 at 10 kΩ and use the following equation to determine R2:

Eq. 6 $$R2(k\Omega) = R1 \times \left(\frac{V_{TRACK}}{RDIV \times V_{OUT}} - 1 \right)$$

R2 must be chosen so that the CS_VTRK input does not exceed 1.2 V.

As seen in Eq. 5, if the resistor-divider ratio from R1//R2 is chosen such that it is equal to the operational RDIV, the output voltage follows the tracking voltage coincidentally. For all other cases, the output voltage follows a ratiometric tracking. These two modes of tracking are further described below.

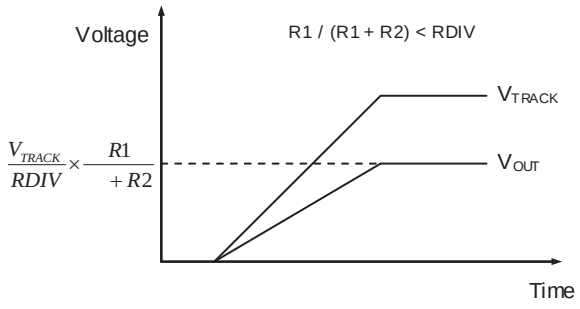
1. Coincident tracking. Output voltage is ramped at the same rate as the VTRACK voltage. To achieve coincident tracking the desired output voltage should be set by the PMBus command VOUT_COMMAND. R2 should be set so that R2 = R1 / RDIV – R1. The output will stop ramping when the VOUT_COMMAND level is reached. Since the voltage at the CS_VTRK pin must be below 1.2 V, coincident tracking will not be possible in all cases. A higher R2 value may be required, giving a ratiometric tracking instead.



Coincident Voltage Tracking

Example:
External VTRACK = 3.3 V
Target VOUT = 2.5 V
R1 = 10 kΩ
VOUT_COMMAND = 2.5 V => RDIV = 0.31597
R2 = 10 / 0.31597– 10 = 21.6 kΩ

2. Ratiometric tracking. Output voltage is ramped at a rate that is a percentage of the VTRACK voltage. To achieve ratiometric tracking, R2 should be set according to Eq. 6 with VOUT being the desired output voltage. The PMBus command VOUT_COMMAND should be set equal to or higher than the output voltage given by Eq. 5, or not being set at all giving the default VOUT_COMMAND value 5.25 V. Since the target voltage level is decided by the R1//R2 divider there will be a small regulation inaccuracy due to the tolerance of the resistors. Note also that VOUT will be higher than VTRACK if R1 / (R1 + R2) > RDIV.



Ratiometric Voltage Tracking

Example:
External VTRACK = 3.3 V
Target VOUT = 1.3 V
VOUT_COMMAND not set => RDIV = 0.20272
R1 = 10 kΩ

Eq. 7 => $$R2 = 10 \times \left(\frac{3.3}{0.20272 \times 1.3} - 1 \right) = 115 k\Omega$$

During voltage tracking compensation calibration is triggered when the output voltage is above 450 mV and stable within a 100 mV window for two consecutive measurements at 10 ms intervals. When calibration is complete, the power good (PG) output is asserted. The PG output remains asserted until the output voltage falls below 450 mV, as verified at 10 ms intervals. For this reason, the PG output may remain high for as much as 10 ms after the output voltage has fallen below 450 mV.

When voltage tracking is enabled the output over voltage protection limit is set 12% above VOUT_COMMAND as default. This limit may be reconfigured using the PMBus command VOUT_OV_FAULT_LIMIT. Output under voltage protection is not functional in tracking mode.

Soft-start parameters TON_DELAY and TON_RISE are not functional in tracking mode and will be set to their minimum values to prevent interference with tracking. TOFF_DELAY and TOFF_FALL can be used if soft-stop is enabled. In such case the output voltage will follow the least of the output levels given by the soft-stop parameters and the tracking equations.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified VI.

The product is tested on a 254 x 254 mm, 35 µm (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

Proper cooling of the product can be verified by measuring the temperature at positions P1, P2 and P3. The temperature at these positions should not exceed the max values provided in the table below. Note that the max value is the absolute maximum rating (non destruction) and that the electrical Output data is guaranteed up to TP1 +95°C.

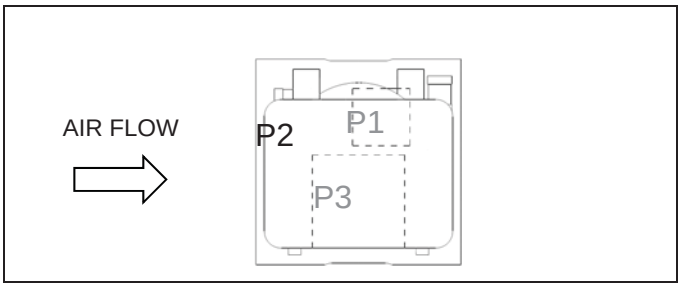
Definition of Product Operating Temperature

The product operating temperature is used to monitor the temperature of the product. Proper thermal conditions can be verified by measuring the temperature at positions P1, P2 and P3. The temperature at these position (TP1,TP2, TP3) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology.

Position	Description	Max Temperature
P1	T3, FET Reference point	125°C *
P2	L1, Inductor	125°C * (115°C **)
P3	N1, Control circuit	115°C *

* A guard band of 5 °C is applied to the maximum recorded component temperatures when calculating output current derating curves.

** See section Alternative thermal verification.



Temperature positions and air flow direction. Top view.

Definition of Reference Temperature TP1

The reference temperature is used to monitor the temperature limits of the product. Temperature above maximum TP1, measured at the reference point P1 is not allowed and may cause degradation or permanent damage to the product. TP1 is also used to define the temperature range for normal operating conditions. TP1 is defined by the design and used to guarantee safety margins, proper operation and high reliability of the product.

Alternative Thermal Verification

Since it is difficult to access positions P1 and P3 of the product, measuring the temperature at only position P2 is an alternative method to verify proper thermal conditions. If measuring only TP2 the maximum temperature of P2 must be lowered since in some operating conditions TP1 will be higher than TP2. Using a temperature limit of 115°C for TP2 will make sure that the temperatures at all points P1, P2 and P3 stay below their maximum limits.

Over Temperature Protection (OTP)

The internal temperature of the product is continously monitored at position P3. When the internal temperature rises above the configured threshold level the product will respond as configured. The product can respond in a number of ways as follows:

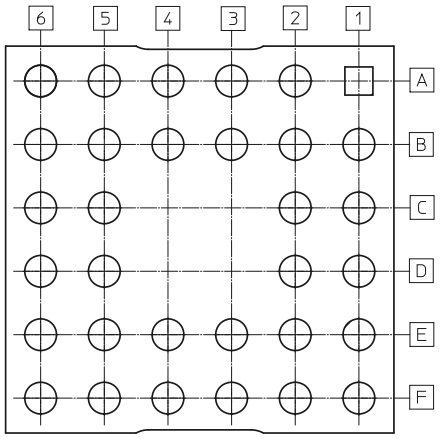
1. Continue operating without interruption (this could result in permanent damage to the product).
2. Continue operating for a given delay period, followed by an output voltage shutdown if the fault still exists.
3. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus or the output voltage is re-enabled.
4. Immediate shutdown of output voltage while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

Default response is 4. The OTP protection uses hysteresis so that the fault exists until the temperature has fallen to a certain level (OT_WARN_LIMIT) below the fault threshold. The default OTP threshold and hysteresis are specified in Electrical Characteristics.

The OTP limit, hysteresis and response can be reconfigured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

The product also incorporates a non-configurable hard-coded thermal shutdown associated with the temperature monitored at position P3 to ensure long-term flash-memory integrity. See Electrical Characteristics.

Connections



Pin layout, bottom view.

The table below gives a brief description of the functionality of each pin. A more detailed description can be found in the different subsections of the Operating Information section.

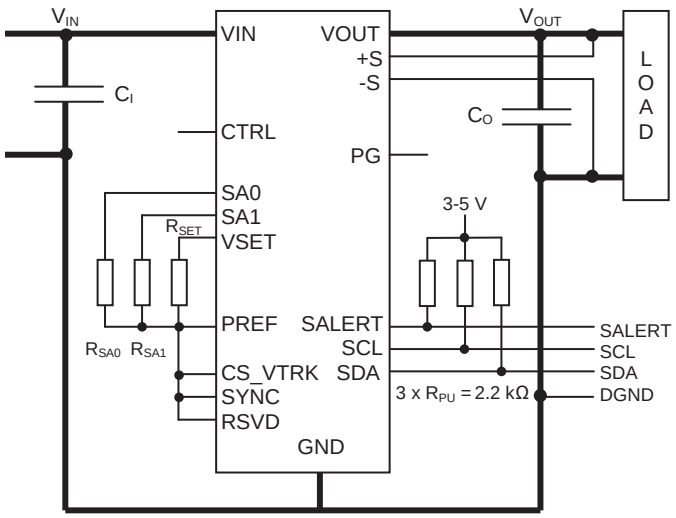
Pin	Designation	Function
1A, 1B, 2A, 2B, 2C, 2D	VOUT	Output Voltage
3A, 3B, 4A, 4B, 5A, 5B	GND	Power Ground
5C, 6A, 6B, 6C	VIN	Input Voltage
1C	+S	Positive sense. Connect to output voltage close to the load
1D	-S	Negative sense. Connect to power ground close to the load.
1E	PG	Power Good output. Asserted high when the product is ready to provide regulated output voltage to the load. Open drain. See section Power Good.
1F	SA0	PMBus address pin strap. Used with external resistors to assign a unique PMBus address to the product. See section PMBus Interface.
3E	SA1	
2F	VSET	Output voltage pin strap. Used with external resistor to set the nominal output voltage or to select tracking mode. See section Output Voltage Adjust using Pin-strap Resistor.
3F	PREF	Pin-strap reference. Ground reference for pin-strap resistors.
6D	CTRL	Remote Control. Can be used to enable/disable the output voltage of the product. See section Remote Control.
2E	SYNC	External switching frequency synchronization input. See section Synchronization.
5F	SALERT	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault.
6E	SDA	PMBus Data. Data signal for PMBus communication. See section PMBus Interface.
6F	SCL	PMBus Clock. Clock for PMBus communication. See section PMBus Interface.
4F	CS_VTRK	Voltage Tracking input. Allows for tracking of output voltage to an external voltage. See section Voltage Tracking. In normal operation when tracking is not used, this pin must be connected to PREF.
4E	RSVD	Reserved. Connect to PREF.
5D, 5E	NC	No connection

Unused Pins

Unused pins should be connected according to the table below. Note that connection of CS_VTRK to PREF is required for normal standalone operation. VSET should always have a pin strap resistor.

Unused Pin	Connection
CS_VTRK	PREF. Required for normal operation
CTRL	Open (pin has internal pull-up)
RSVD	PREF or pulled down to PREF
SYNC	PREF or pulled down to PREF
SA0	PREF or Open
SA1	PREF or Open
SDA	Pull-up resistor to voltage > 2 V
SCL	Pull-up resistor to voltage > 2 V
PG	Open
SALERT	Open

Typical Application Circuit



Typical standalone operation with PMBus communication.

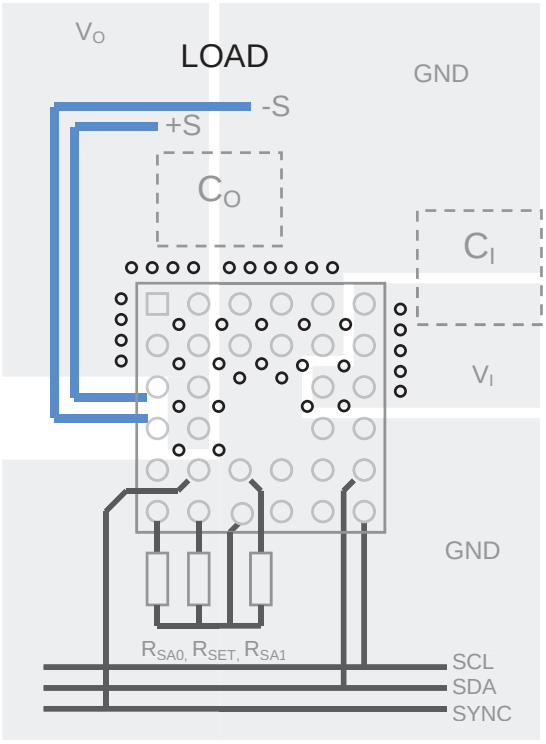
PCB Layout Consideration

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

Further layout recommendations are listed below.

- The pin strap resistors, RSET, and RSA0/RSA1 should be placed as close to the product as possible to minimize loops that may pick up noise.
- Avoid current carrying planes under the pin strap resistors and the PMBus signals.
- The capacitors CI should be placed as close to the input pins as possible.
- The capacitors CO should be placed close to the load.
- The point of output voltage sense should be “downstream” of CO according to figure below.
- Care should be taken in the routing of the connections from the sensed output voltage to the S+ and S– terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields.
- If possible use planes on several layers to carry VI, VO and GND. There should be a large number of vias close to the VIN, VOUT and GND pads in order to lower input and output impedances and improve heat spreading between the product and the host board.



Layout guidelines

PMBus Interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I2C or SMBus host device. In addition, the product is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_P C_p \leq 1\mu s$$

where Rp is the pull-up resistor value and Cp is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.7 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

Monitoring via PMBus

It is possible to monitor a wide variety of parameters through the PMBus interface. Fault conditions can be monitored using the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. It is also possible to continuously monitor one or more of the power conversion parameters including but not limited to the following:

- Input voltage (READ_VIN)
- Output voltage (READ_VOUT)
- Output current (READ_IOUT)
- Internal junction temperature (READ_TEMPERATURE_1)
- Switching frequency (READ_FREQUENCY)
- Duty cycle (READ_DUTY_CYCLE)

Reading Set Parameters

To clearly display the true performance of the product, PMBus command reads of set levels, limits and timing parameters will return the internally used values. For this reason, due to rounding or internal representation in the controller of the product, there may be a difference between written and read value of a PMBus command. This applies to PMBus commands of type Linear or VoutLinear. When verifying write transactions, tolerances according to the table below can be used.

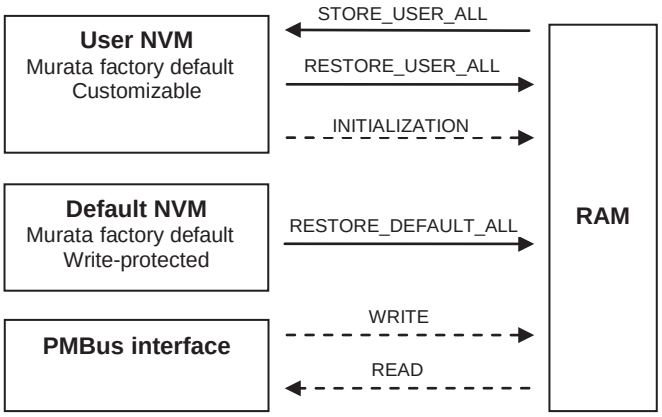
PMBus Command	Read Back Accuracy
COMP_MODEL	±0
VIN_ON	±0.1 V
VIN_OFF	
VIN_UV_FAULT_LIMIT	
VIN_OV_FAULT_LIMIT	
IOUT_OC_FAULT_LIMIT	±0.1 A
TON_DELAY	±0.3 ms
TOFF_DELAY	
TON_RISE	±0.4 ms
TOFF_FALL	
VOUT_COMMAND	±0.001 V
VOUT_MAX	
VOUT_MARGIN_HIGH	
VOUT_MARGIN_LOW	
VOUT_TRANSITION_RATE	±0.5 V
VOUT_OV_FAULT_LIMIT	±0.01 V
VOUT_UV_FAULT_LIMIT	
POWER_GOOD_ON	
POWER_GOOD_OFF	

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the supported PMBus commands; the Default NVM and the User NVM.

The Default NVM is pre-loaded with Murata Power Solutions factory default values. The Default NVM is write-protected and can be used to restore the Murata Power Solutions factory default values through the command RESTORE_DEFAULT_ALL. The RESTORE_DEFAULT_ALL command will load a nominal output level of 0 V. Therefore, after a RESTORE_DEFAULT_ALL command is sent, the input voltage must be cycled in order to load correct output voltage level according to VSET pin-strap resistor (see section Startup procedure).

The User NVM is pre-loaded with Murata Power Solutions factory default values. The User NVM is writable and open for customization. The values in the User NVM are loaded during initialization whereafter commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.



Protecting Commands

The user may write-protect specific PMBus commands in the User NVM by following the steps below.

1. Enter the default password 0x0000 through the command USER_PASSWD. After the correct password is entered, SECURITY_LEVEL will read back 0x01 instead of default 0x00.
2. If desired, define a new password by writing it to the USER_LOCK command.
3. Define which commands should be locked by using the 256 bit command USER_CONF. Setting bit X will write-protect the PMBus command with code X.
4. Send command STORE_USER_ALL.
5. Cycle the input voltage.

Software Tools for Design and Production

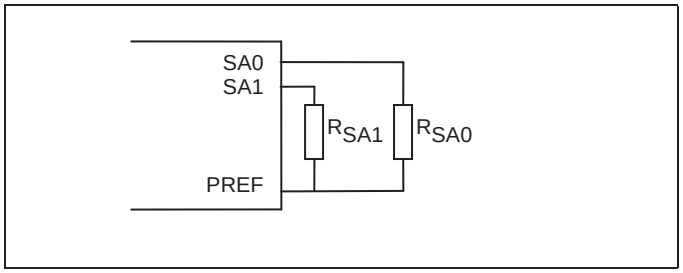
Murata Power Solutions provides software tools for configuration and monitoring of this product via the PMBus interface.

For more information please contact your local Murata Power Solutions sales representative.

PMBus Addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the table and figure below. Note that five different values of RSA1 produce the same address. Recommended resistor values for hard-wiring PMBus addresses are shown in the table. 1% tolerance resistors are required. The configurable PMBus addresses range from 0x0A to 0x7F. In total 118 device address combinations are provided.

	RSA1 [kΩ]				
	≤ 4.22	5.11	6.19	7.15	8.25
	9.53	11.0	12.7	14.7	17.8
	21.5	26.1	31.6	38.3	44.2
	51.1	59.0	68.1	86.6	115
RSA0 [kΩ]	140	169	205	237	≥ 274
≤ 4.22	0x0A	0x22	0x3A	0x52	0x6A
5.11	0x0B	0x23	0x3B	0x53	0x6B
6.19	0x0C	0x24	0x3C	0x54	0x6C
7.15	0x0D	0x25	0x3D	0x55	0x6D
8.25	0x0E	0x26	0x3E	0x56	0x6E
9.53	0x0F	0x27	0x3F	0x57	0x6F
11.0	0x10	0x28	0x40	0x58	0x70
12.7	0x11	0x29	0x41	0x59	0x71
14.7	0x12	0x2A	0x42	0x5A	0x72
17.8	0x13	0x2B	0x43	0x5B	0x73
21.5	0x14	0x2C	0x44	0x5C	0x74
26.1	0x15	0x2D	0x45	0x5D	0x75
31.6	0x16	0x2E	0x46	0x5E	0x76
38.3	0x17	0x2F	0x47	0x5F	0x77
44.2	0x18	0x30	0x48	0x60	0x78
51.1	0x19	0x31	0x49	0x61	0x79
59.0	0x1A	0x32	0x4A	0x62	0x7A
68.1	0x1B	0x33	0x4B	0x63	0x7B
86.6	0x1C	0x34	0x4C	0x64	0x7C
115	0x1D	0x35	0x4D	0x65	0x7D
140	0x1E	0x36	0x4E	0x66	0x7E
169	0x1F	0x37	0x4F	0x67	0x7F
205	0x20	0x38	0x50	0x68	0x7F
≥ 237	0x21	0x39	0x51	0x69	0x7F



Schematic of connection of address resistor.

Optional PMBus Addressing

The user may leave SA0/SA1 open or shorted to PREF.

Shorting SA0/SA1 to PREF corresponds to RSA0/RSA1 ≤ 4.22 kΩ in the address table above.

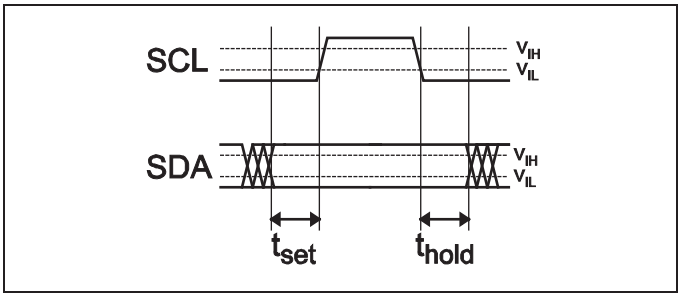
Leaving SA0/SA1 open corresponds to RSA0/RSA1 ≥ 274 kΩ in the address table above.

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	General Call Address / START byte
0x01	CBUS address
0x02	Address reserved for different bus format
0x03 - 0x07	Reserved for future use
0x08	SMBus Host
0x09 - 0x0B	Assigned for Smart Battery
0x0C	SMBus Alert Response Address
0x28	Reserved for ACCESS.bus host
0x2C - 0x2D	Reserved by previous versions of the SMBus specification
0x37	Reserved for ACCESS.bus default address
0x40 - 0x44	Reserved by previous versions of the SMBus specification
0x48 - 0x4B	Unrestricted addresses
0x61	SMBus Device Default Address
0x78 - 0x7B	10-bit slave addressing
0x7C - 0x7F	Reserved for future use

I2C/SMBus – Timing



Setup and hold times timing diagram

The setup time, tset, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time thold, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification, for SMBus electrical and timing requirements.

The bus-free time (time between STOP and START packet) according to Electrical Specification must be followed.

The product supports PEC (Packet Error Checking) according to the SMBus specification.

In operation cases according to the list below the product's controller will be executing processor-intensive tasks and may not respond to PMBus commands.

- During the presence of an overcurrent fault.
- Just after the output voltage has been enabled. It is recommended to wait until PG is asserted (or the equivalent time) before sending commands.
- When sending subsequent commands to the same unit it is recommended to insert additional delays after write transactions according to the table below.

PMBus Command	Delay after Write before Additional Command
STORE_USER_ALL	500 ms
STORE_DEFAULT_ALL	
DEADTIME_GCTRL	
USER_CONF	350 ms
MANUF_CONF	
RESTORE_USER_ALL	10 ms
RESTORE_DEFAULT_ALL	
FREQUENCY_SWITCH	
VOUT_DROOP	0.5 ms
IOUT_CAL_GAIN	
ADAPTIVE_MODE	
FEEDBACK_EFFORT	
LOOP_CONFIG	
COMP_MODEL	
ZETAP	

PMBus Commands

The product is PMBus compliant. The following table lists all the implemented PMBus read commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

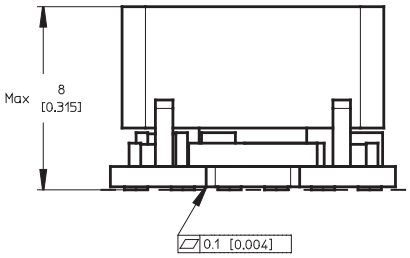
Designation	Code	Impl*
Standard PMBus Commands		
Control Commands		
PAGE	00h	No
OPERATION	01h	Yes
ON_OFF_CONFIG	02h	Yes
WRITE_PROTECT	10h	Yes
Output Commands		
CAPABILITY (read only)	19h	Yes
VOUT_MODE (read Only)	20h	Yes
VOUT_COMMAND	21h	Yes
VOUT_TRIM	22h	Yes
VOUT_CAL_OFFSET	23h	Yes
VOUT_MAX	24h	Yes
VOUT_MARGIN_HIGH	25h	Yes
VOUT_MARGIN_LOW	26h	Yes
VOUT_TRANSITION_RATE	27h	Yes
VOUT_DROOP	28h	Yes
MAX_DUTY	32h	No
FREQUENCY_SWITCH	33h	Yes
VIN_ON	35h	Yes
VIN_OFF	36h	Yes
IOUT_CAL_GAIN	38h	Yes
IOUT_CAL_OFFSET	39h	Yes
VOUT_SCALE_LOOP	29h	No
VOUT_SCALE_MONITOR	2Ah	No
COEFFICIENTS	30h	No
Fault Limit Commands		
POWER_GOOD_ON	5Eh	Yes
POWER_GOOD_OFF	5Fh	Yes
VOUT_OV_FAULT_LIMIT	40h	Yes
VOUT_OV_WARN_LIMIT	42h	No
VOUT_UV_WARN_LIMIT	43h	No

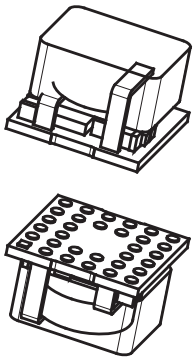
Designation	Code	Impl*
VOUT_UV_FAULT_LIMIT	44h	Yes
IOUT_OC_FAULT_LIMIT	46h	Yes
IOUT_OC_LV_FAULT_LIMIT	48h	No
IOUT_OC_WARN_LIMIT	4Ah	No
IOUT_UC_FAULT_LIMIT	4Bh	No
OT_FAULT_LIMIT	4Fh	Yes
OT_WARN_LIMIT	51h	Yes
UT_WARN_LIMIT	52h	No
UT_FAULT_LIMIT	53h	No
VIN_OV_FAULT_LIMIT	55h	Yes
VIN_OV_WARN_LIMIT	57h	No
VIN_UV_WARN_LIMIT	58h	No
VIN_UV_FAULT_LIMIT	59h	Yes
Fault Response Commands		
VOUT_OV_FAULT_RESPONSE	41h	Yes
VOUT_UV_FAULT_RESPONSE	45h	Yes
OT_FAULT_RESPONSE	50h	Yes
UT_FAULT_RESPONSE	54h	No
VIN_OV_FAULT_RESPONSE	56h	Yes
VIN_UV_FAULT_RESPONSE	5Ah	Yes
IOUT_OC_FAULT_RESPONSE	47h	Yes
IOUT_OC_LV_FAULT_RESPONSE	49h	No
IOUT_UC_FAULT_RESPONSE	4Ch	No
TON_MAX_FAULT_RESPONSE	63h	Yes
Time setting Commands		
TON_DELAY	60h	Yes
TON_RISE	61h	Yes
TOFF_DELAY	64h	Yes
TOFF_FALL	65h	Yes
TON_MAX_FAULT_LIMIT	62h	Yes
Status Commands (Read Only)		
CLEAR_FAULTS	03h	Yes
STATUS_BYTE	78h	Yes
STATUS_WORD	79h	Yes
STATUS_VOUT	7Ah	Yes
STATUS_IOUT	7Bh	Yes
STATUS_INPUT	7Ch	Yes
STATUS_TEMPERATURE	7Dh	Yes
STATUS_CML	7Eh	Yes
STATUS_MFR_SPECIFIC	80h	Yes
Monitor Commands (Read Only)		
READ_VIN	88h	Yes
READ_IIN	89h	No
READ_VOUT	8Bh	Yes
READ_IOUT	8Ch	Yes
READ_TEMPERATURE_1	8Dh	Yes
READ_TEMPERATURE_2	8Eh	Yes
READ_FAN_SPEED_1	90h	No
READ_DUTY_CYCLE	94h	Yes
READ_FREQUENCY	95h	Yes
READ_POUT	96h	No
READ_PIN	97h	No
Group Commands		
INTERLEAVE	37h	Yes
PHASE_CONTROL	F0h	No

Designation	Code	Impl*
Identification Commands		
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes
MFR_MODEL	9Ah	Yes
MFR_REVISION	9Bh	Yes
MFR_LOCATION	9Ch	Yes
MFR_DATE	9Dh	Yes
MFR_SERIAL	9Eh	Yes
IC_DEVICE_ID	ADh	Yes
IC_DEVICE_REV	AEh	Yes
Supervisory Commands		
STORE_DEFAULT_ALL	11h	Yes
RESTORE_DEFAULT_ALL	12h	Yes
STORE_USER_ALL	15h	Yes
RESTORE_USER_ALL	16h	Yes
Product Specific Commands		
ADAPTIVE_MODE	D0h	Yes
FEEDBACK_EFFORT	D3h	Yes
LOOP_CONFIG	D5h	Yes
TEST_MODE	D9h	Yes
COMP_MODEL	DBh	Yes
STRAP_DISABLE	DCh	Yes
MANUF_CONF	E0h	Yes
MANUF_LOCK	E1h	Yes
MANUF_PASSWD	E2h	Yes
USER_CONF	E3h	Yes
USER_LOCK	E4h	Yes
USER_PASSWD	E5h	Yes
SECURITY_LEVEL	E6h	Yes
DEADTIME_GCTRL	E7h	Yes
ZETAP	E8h	Yes

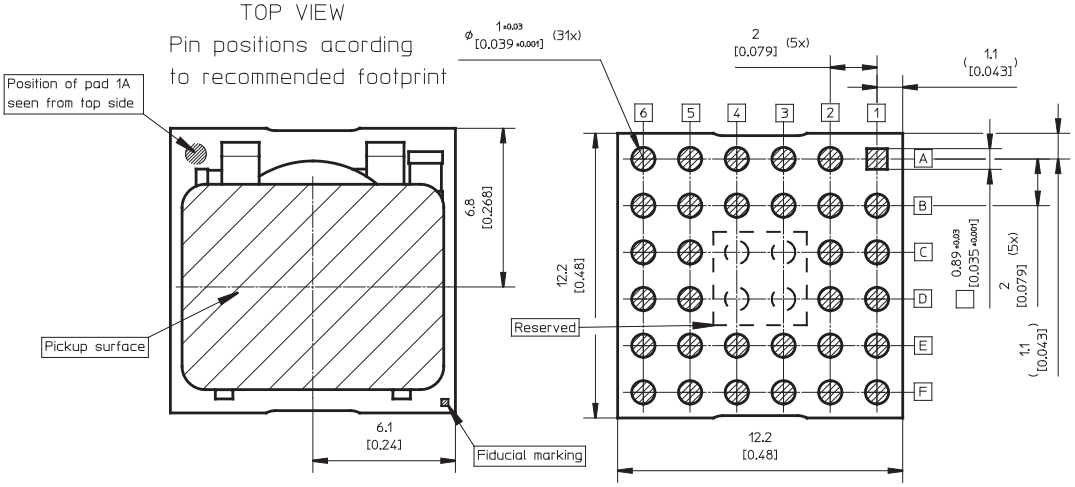
*Impl stands for Implemented.

MECHANICAL SPECIFICATIONS

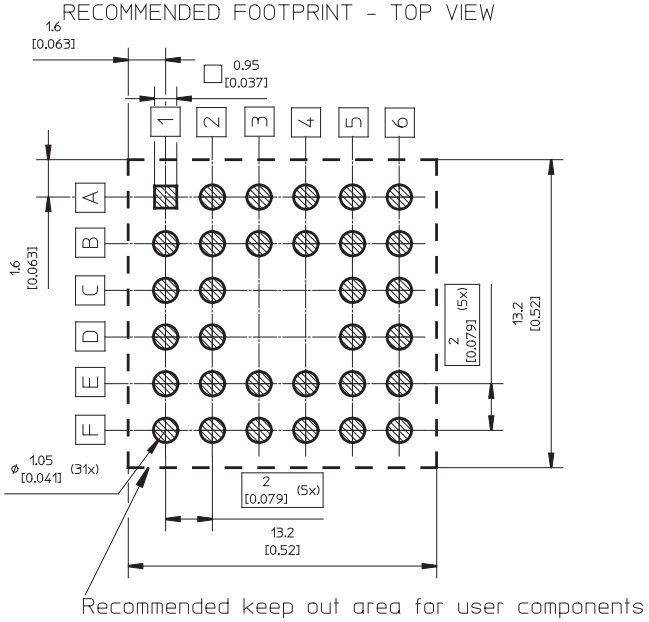




TOP VIEW
Pin positions acording
to recommended footprint



RECOMMENDED FOOTPRINT - TOP VIEW



Weight: Typical 3.2 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.5 mm [0.02]
x.xx±0.25 mm [0.01]
(not applied on footprint or typical values)

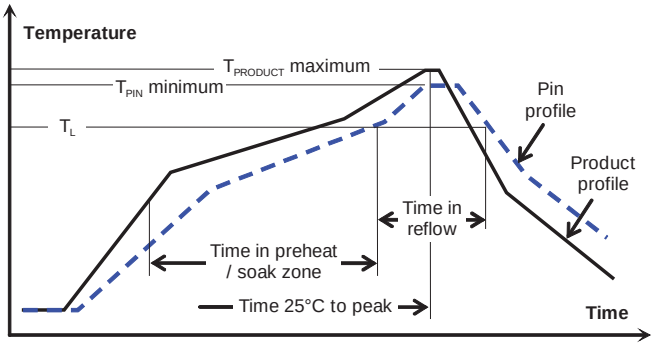
Soldering Information - Surface Mounting

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up (TPRODUCT)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above TL		30 s	30 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number C1 or D1 are chosen as reference location for the minimum pin temperature recommendation since these will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (TPIN) in excess of the solder melting temperature, (TL, 183°C for Sn63Pb37) for more than 30 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (TPIN) in excess of the solder melting temperature (TL, 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PCB near pin A2 or A5 is chosen as reference locations for the maximum (peak) allowed product temperature (TP_{RODUCT}) since these will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J STD 020C.

During reflow TP_{RODUCT} must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

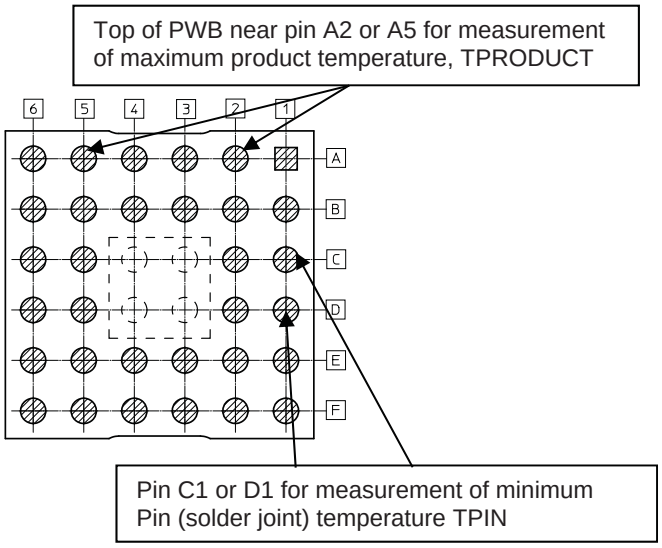
During reflow TP_{RODUCT} must not exceed 260 °C at any time.

Dry Pack Information

Surface mounted versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J STD 033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J STD 033.

Thermocoupler Attachment



Surface Mount Assembly and Repair

The LGA of the product require particular care during assembly since the LGA´s are hidden between the host board and the product's PCB. Special procedures are required for successful rework of these products.

Assembly

Automatic pick and place equipment should be used to mount the product on the host board. The use of a vision system, utilizing the fiducials on the bottom side of the product, will ensure adequate accuracy. Manual mounting of solder bump products is not recommended.

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Repair

For a successful repair (removal and replacement) of a LGA product, a dedicated rework system should be used. The rework system should preferably utilize a reflow station and a bottom side heater might also be needed for the operation.

The product is an open frame design with a pick up surface on a large central component (in this case the choke). This pick up surface can be used for removal of the module provided that it is glued against module PCB before removal to prevent it from separating from the module PCB.

Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
Material	PS, antistatic
Surface resistance	< 107 Ohm/square
Bakeability	The tape is not bakable
Tape width, W	24 mm [0.94 inch]
Pocket pitch, P1	20 mm [0.79 inch]
Pocket depth, K0	8.6 mm [0.339 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	280 products /reel
Reel weight	1160 g/full reel